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A 2.4GHZ DIRECT CONVERSION MIXER WITH OFFSET CANCELLATION.

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Dynamic DC offset is one of the biggest problems preventing the implementation of single chip receivers. This thesis presents a 2.4GHz downconversion mixer designed to work with adaptive DC offset cancellation for a fully integrated direct conversion receiver. Offset can be removed by dynamically changing the PFET load bias in a Gilbert Cell type mixer. A dual-loop algorithm, which was developed in separate work, controls a current-steering DAC that dynamically changes the PFET load bias of the mixer. The mixer has a gain of 8dB, an IIP3 of 17dBm, and a noise figure of 15dB. In addition a CMOS RF Front-End incorporating the offset cancellation mixer is presented that meets the specifications for Bluetooth.

A 2.4GHZ DIRECT CONVERSION MIXER WITH OFFSET CANCELLATION

by

Hardy Schmidbauer

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Hardy Schmidbauer, Author

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1.0 INTRODUCTION

1.1 Next Generation Wireless Systems

Short-range wireless networking is seen as the next explosive market for many applications and technologies. As the markets and standards for personal consumer electronics, i.e., Bluetooth, HomeRF, and IEEE 802.11 develop, the demand for low cost, low power receivers will increase. Experts believe that to make these systems marketable IC manufactures need to achieve a $5.00 price target per Tx/Rx chip. This constraint is forcing designers to strive for a single-chip solution that minimizes cost and power consumption while maximizing features and performance. Consequently, designers are forced to consider different architectures and fabrication process technologies.

1.2 Competing WLAN Standards

All home wireless local-area-networks (WLAN) standards -- Bluetooth, HomeRF, and IEEE 802.11-- operate in the 2.4GHz industrial-scientific medical spectrum band. Bluetooth is the name of the specifications for small-form factor, low-cost, short-range radio links between PCs, mobile phones, and other personal portable devices. It was developed by PC and mobile phone manufactures as a low-cost wireless voice/data cable replacement. IEEE 802.11 was developed for enterprise LAN applications to

provide a wireless extension to Ethernet LANs. PC manufactures developed Home RF to simplify and reduce the cost of 802.11 for home use. The major difference between the standards is that HomeRF and 802.11 add connection or access points in their primary configurations to control LAN operation. In Bluetooth, ad-hoc networks are developed consisting of up to eight nodes, where each node may be a master or a slave [34].

Currently, Bluetooth seems to be the dominant emerging standard for home personal use. Originally, Bluetooth was intended for communication within 10 meters with a modulation rate of 1Mb/s. Recently, the standard has been extended to communication within 50 meters using a modulation rate of 50 Mb/s. Bluetooth uses frequency-hopping spread-spectrum with a hop rate of 1600-hops/s. Key specifications for the receiver are a –70dBm sensitivity, 1-dB point of –20dBm, and an IIP3 point of -16dBm [42].

1.3 Process Technologies

The high-volume and low-cost characteristics of CMOS make it attractive when considering a single integrated chip solution, but with a standard CMOS process it is difficult to design a high performance system. The highest performance technology today is Si-Germanium (SiGe), but the cost of this process makes it unmarketable for home use. The most commonly used technology for home networking applications is BiCMOS, which provides a tradeoff between cost and performance [34]. Also being considered is Silicon-On-Insulator CMOS, or SOI-CMOS, which allows for better passive devices than standard CMOS. As in BiCMOS, the boost in performance of

SOI-CMOS will translate as increased cost. In this work a CMOS process is utilized to take advantage of is desirable characteristics.

1.4 Receiver Architectures

Most of today's receivers on the market use a conventional superheterodyne architecture (see Figure 1-1).

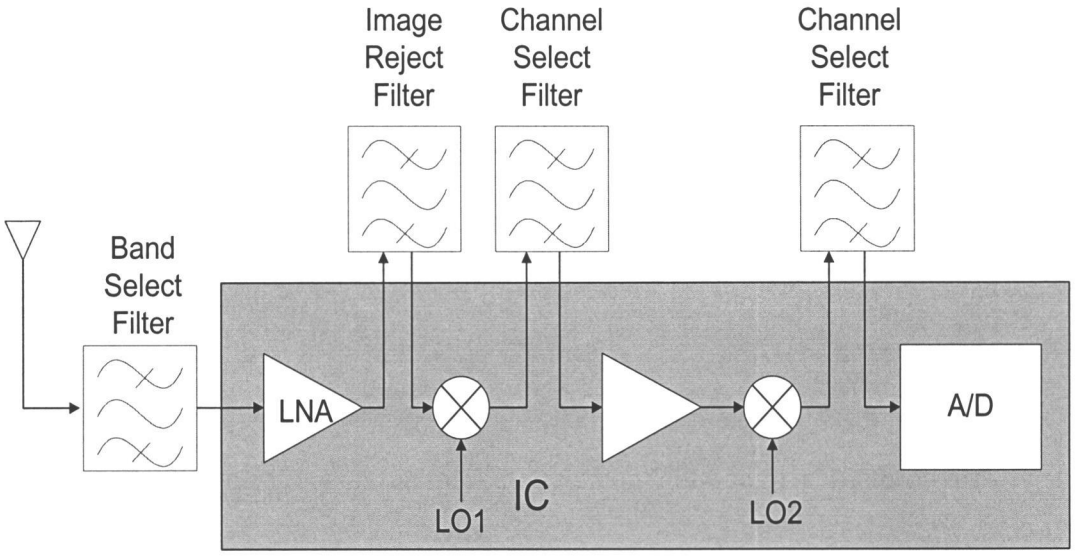

Figure 1-1: Basic superheterodyne architecture

This type of architecture provides excellent selectivity and sensitivity. The architecture has many advantages but it also has many disadvantages. As seen in Figure 1-1, filtering a narrow channel at high frequencies with large interferes requires high Q off-chip filters. Due to the presence of off-chip components the LNA must drive a low impedance node, which complicates the design. The main problem associated with this

architecture is the problem of image. The image frequency is converted to the same frequency as the desired channel. If the band of interest is centered around $\omega_1 = \omega_{LO} - \omega_{IF}$, then the image frequency is at $\omega_{im} = \omega_{LO} + \omega_{IF}$. A high IF leads to substantial image rejection while a low IF allows for greater interferer suppression [2]. These trade-offs must be considered when selecting the intermediate frequencies. The complexity, high cost, and the need for a large number of external components make this type of architecture unattractive for home networking applications.

Homodyne receivers directly convert the desired RF channel to baseband in one step, as shown in Figure 1-2.

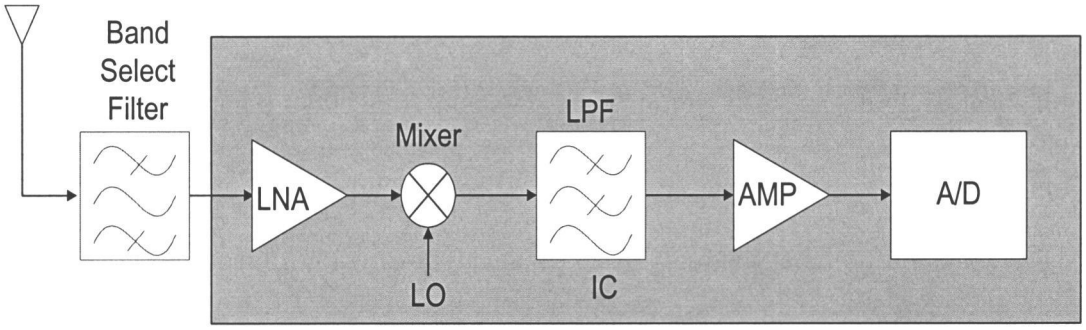

Figure 1-2: Homodyne receiver architecture

The simplicity of this architecture gives it three critical advantages over the heterodyne architecture. First, the problem of the image is eliminated because $\omega_{IF} = 0$. Second, the need for expensive off-chip filters is eliminated giving way to a completely integrated system [2], [4], [5]. Third, far fewer external components are needed; therefore, it consumes less power and costs less to manufacture, which are the primary

specifications for portable devices. The homodyne architecture has many benefits, but it also has a number of problems not found in heterodyne. The downconverted spectrum is centered at zero frequency, thus offset voltages corrupt the signal and can saturate downstream stages. There are two types of offsets that can occur, static and dynamic. Static offsets come from several sources. First, they are caused by the Local Oscillator (LO) coupling through the substrate to the mixer or LNA input, see Figure 1-3. This leakage signal is now mixed with the LO signal, creating a DC offset as shown in (1.1). When two signals of the same frequency are mixed, a DC term and a double frequency term are created. It is the DC term that creates a problem

$$(A\cos(\omega_{LO}t))(A\cos(\omega_{LO}t)) = \frac{A^2}{2} + \frac{A^2}{2}\cos(2\omega_{LO}t) \quad (1.1)$$

Second, any mismatch between the differential legs in the mixer will create a static offset [2], [4], [5]. Dynamic offsets arise from several sources. First a strong in-band interferer may similarly be coupled to the LO port and self mixed creating a DC offset.

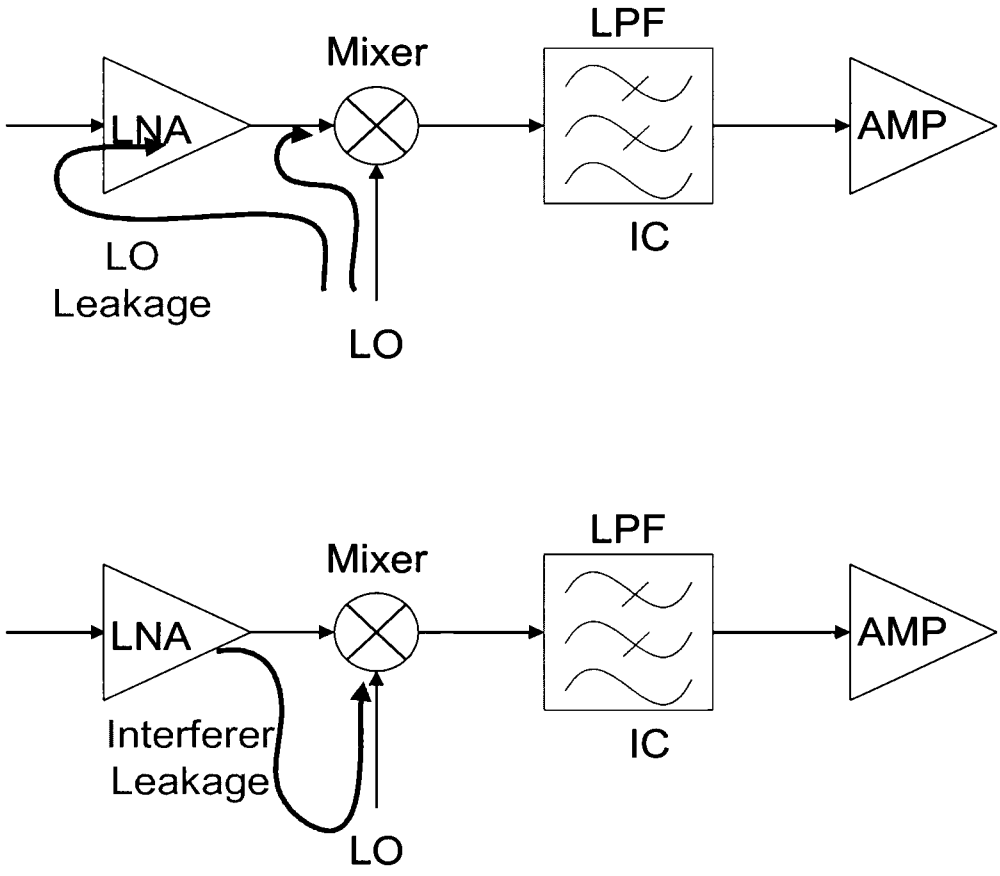

Figure 1-3: Static and dynamic offsets in direct conversion

Second, a user's LO may couple to the antenna radiate out and be reflected back off external objects, as shown in Figure 1-4. These time-varying offsets are very difficult to track and correct for.

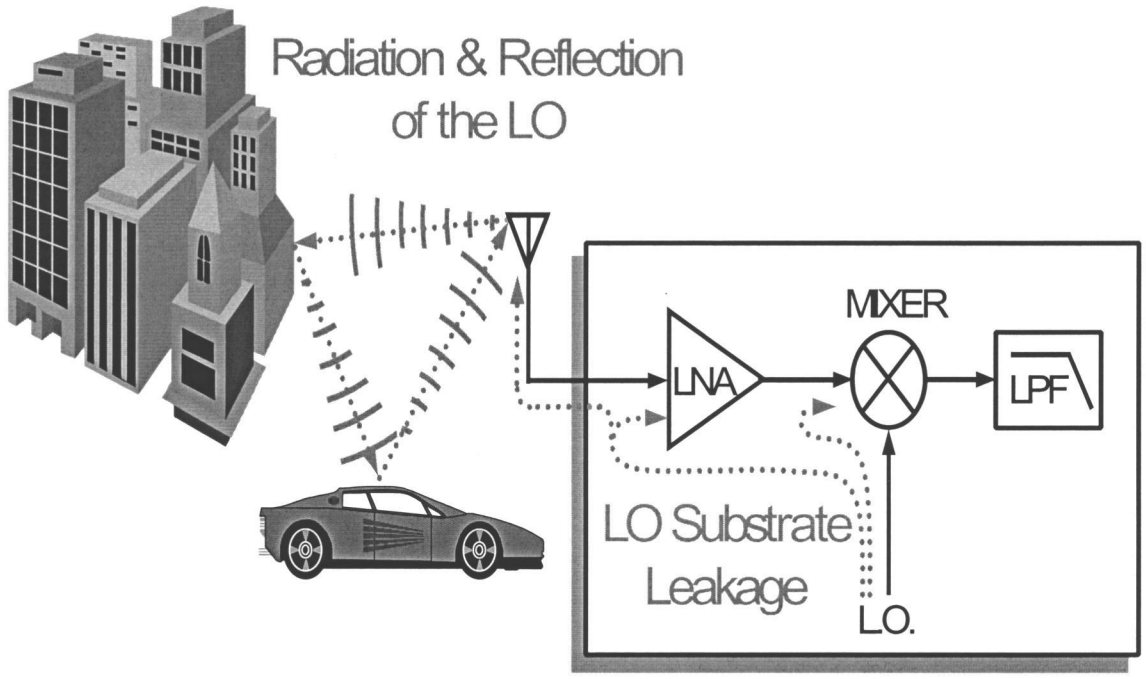

Figure 1-4: Dynamic offsets in direct conversion

Closely associated with the offset problem is second order distortion, which is characterized by IIP2. Ideally, a double-balanced mixer would have an infinite IIP2 due to its perfect cancellation of second order products. An offset or mismatch between the differential legs will cause this cancellation to be imperfect, creating second order distortion. Low frequency noise or flicker noise (1/f noise) is also problematic for direct conversion receivers implemented in CMOS. Flicker noise can substantially corrupt weak baseband signals. Additionally, channel selection in a homodyne architecture is more diffucult than in heterodyne. Active low pass filters do not reject out-of-band interferers as well as their passive counterparts, and exhibit a much more severe noise-linearity-power tradeoff [2]. Yet, another problem with the homodyne architecture is I/Q mismatch. Any error in the quadrature LO or mismatch in the I/Q paths will raise

the Bit-Error-Rate (BER). Previous research by Professor John Stonick of OSU has shown that a DSP correction algorithm can correct for gain and phase mismatch errors, greatly improving the BER performance [45].

If the problems that have previously hindered the implementation of direct conversion receivers can be overcome, they would be the ideal architecture for short-range networking applications due to their low cost and completely integrated solution.

1.5 Research Objective

The goal of this research is to develop a mixer and LNA to combat the problem of DC Offsets in the direct conversion architecture. The solution should be completely integrated, to promote the low cost and low power characteristics of the architecture, plus meet the specifications for the emerging home networking standards, such as Bluetooth. To further promote the low cost characteristics of the architecture all circuit design will be done in a standard CMOS process.

2.0 BASIC CONCEPTS AND PERFORMANCE MEASUREMENTS FOR RF RECEIVERS

2.1 Noise Figure

Noise factor (F) is a measure of the noise performance of a system. When the noise factor is expressed in decibels it is called Noise Figure (NF). It is commonly defined as SNR in divided by SNR out, or by the total output noise divided by the output noise due to the input source. For a receiver the input source is considered to be the antenna port. For a simple amplifier with input referred noise-voltage(v_n) and current(i_n), as shown in Figure 2-1, the noise figure is [2] [39]:

$$NF = 10 * \log 10\left(1 + \frac{(v_n + i_n Rs)^2}{4KTRs}\right) \quad (2.1).$$

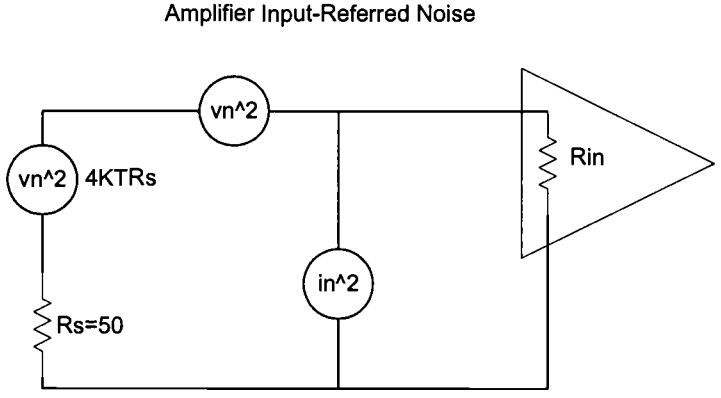

Figure 2-1: Noise figure for a simple amplifier

For a cascade of stages in the receiver chain the overall noise figure is determined from the F and gain of the individual stages, (Figure 2-2).

$$F_{Tot} = F1 + \frac{F2-1}{A1^2} + \frac{F3-1}{(A1^2 * A2^2)} \quad (2.2)$$

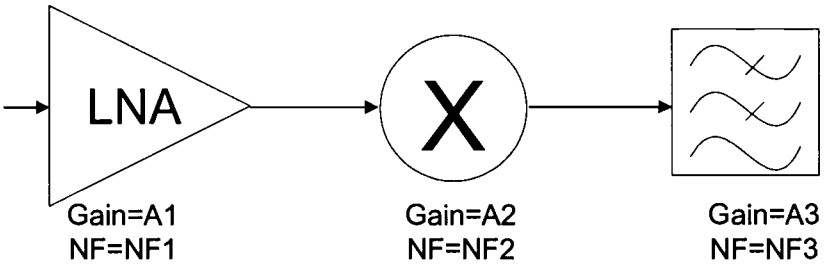

Figure 2-2: Noise figure of cascaded stages

In direct conversion mixers, it is important to differentiate between Double Side Band (DSB) Noise Figure and Single Side Band (SSB) Noise Figure. In a heterodyne architecture, upon downconversion the signal, the noise in the signal band, and the noise in the image band are translated to the IF frequency. Therefore, the theoretical output SNR of the mixer is half the input SNR, or 3dB less. In this architecture the minimum NF is 3dB for a noiseless ideal circuit. Since only a single sideband contributes to the SNR, this is considered a SSB NF calculation. In a homodyne architecture, the signal spectrum lies on both sides of the LO frequency, and there is no image; therefore, the input and output SNR are theoretically equal, 0dB NF. In this architecture the NF is called DSB because the signal lies on both sides of the LO. The SSB noise figure of a mixer is 3dB higher than a DSB noise figure [2] [39].

2.2 IIP3

The input referred third order intercept point, IIP3, is a performance measurement of third order intermodulation products. The IIP3 is the input power level where the power of the third order intermodulation terms equals the theoretical power of the fundamental tone. Intermodulation products are caused by the inherent nonlinearities of analog circuits. This is evident when the output of an amplifier is represented by a power series [1] [40].

$$V_o(t) = a_1 V(t) + a_2 V^2(t) + a_3 V^3(t) \quad , \quad V(t) = A\cos(\omega t) \quad (2.3)$$

The third order intermodulation product, IM3, is measured by a two-tone test using

$$V(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \quad (2.4)$$

By substitution (2.4) into (2.3) for V(t) and collecting terms, it can be seen that the cubic term causes third-order intermodulation products at: $2\omega_1 \pm \omega_2, \omega_1 \pm 2\omega_2$. These components are important because they appear in close proximity to the desired signal ω_1. From (2.3), as A increases the fundamental terms increase proportional to A, while the IM3 products increase proportional to A^3. On a logarithmic plot, the IM3 products grow with a rate or slope of three, while the fundamental grows with a slope of one. The input power where the magnitude of the IM3 products equals the fundamental is defined as the third-order intercept point, or IIP3. Output Referred Third Order Intercept Point (OIP3) is defined as the output power where these lines cross.

As in the case for cascaded noise figure, IIP3 may be approximated for a system from the gain and IIP3 measurements of the individual stages [40]:

$$\frac{1}{(A_{IIP3})^2} = \frac{1}{(A_{IIP3,1})^2} + \frac{a_1^2}{(A_{IIP3,2})^2} + \ldots\ldots \quad (2.5)$$

2.3 IIP2

IIP2 is a similar measurement to IIP3 but instead of measuring the third-order intermodulation products the second order products are used: $\omega_1 \pm \omega_2$. From substituting (2.3) into (2.4), the squared term causes second order intermodulation products, IM2, at $\omega_1 - \omega_2$, and $\omega_1 + \omega_2$. Therefore, two high frequency signals generate a low frequency beat. A low frequency IM2 product generated in the LNA would ideally be upconverted to the LO frequency in the mixer. Although, due to mismatch of devices a finite amount of direct feedthrough is present in a mixer. Therefore, a fraction of the low frequency beat will appear at the output with no frequency translation [5]. This is problematic in a direct conversion architecture, because this low frequency beat is in close proximity to the desired signal. Additionally, the second harmonic of the input signal is mixed with the second harmonic of the LO creating a corrupting signal at baseband [5].

2.4 Sensitivity

Sensitivity is defined as the minimum signal level that produces an acceptable SNR at the output of a system. It is calculated by:

$$Sens = -174dBm/Hz + NF + 10\log10(BW) + SNR_{\min} \quad (2.6)$$

where -174dBm/Hz is the thermal noise at room temp, NF is the overall noise figure of the system, BW is the bandwidth of the system, and $SNR_{\min}$ is the minimum signal-to-noise ratio that is required by the demodulator to maintain a certain BER.

2.5 Dynamic Range

Dynamic range (DR) is commonly described as the ratio of the maximum input signal level the circuit can permit to the minimum input level that the circuit can operate with acceptable signal quality. In RF design, Spurious Free Dynamic Range (SFDR) is used to illustrate DR performance. The upper end of the SFDR is determined by the intermodulation performance and the lower end by the sensitivity. The upper end is more specifically defined as the maximum input level in a two-tone test for which the third-order IM products do not exceed the noise floor.

$$SFDR = \frac{2(P_{IIP3} - F_n)}{3} - SNR_{\min} \quad (2.7)$$

$$F_n = -174dB + NF + 10\log(BW) \quad (2.8)$$

3.0 REVIEW OF RELATED LITERATURE

3.1 Introduction

This chapter presents solutions that have been previously published on the implementation of low-cost, completely integrated radios for home networking. Section 3.2 discusses the different type of architectures used to implement a completely integrated radio. Some authors chose direct conversion, while others have chosen a Low-IF heterodyne architecture. Section 3.3 discusses the offset cancellation schemes proposed by the authors who implemented a direct conversion architecture. Mixer and LNA designs are discussed and analyzed in sections 3.4 and 3.5.

3.2 Architecture Design

Numerous direct conversion radios have been presented [9] [10] [11] [12] [13] [20] [21], each highlighting the advantages discussed in section 1.4 and presenting their own solution to the problems associated with this architecture. Most of these solutions are discussed along with their offset correction technique in section 3.3. Other authors have focused on a low IF architectures, [8] [14] [17], to implement a completely integrated radio.

When first presented with the problem of DC offsets the simplest solution seems to a high-pass filter or AC coupling to the next stage past the mixer. Since, the signal is being converted to baseband, a very low corner frequency is required. Assuming a 10pF coupling capacitor, a 1.6MΩ resistor is needed to create a 10kHz corner frequency. A

1.6MΩ resistor made with typical nwell material would consume a large die area and would exhibit enormous parasitic capacitance to substrate, much greater than 10pF [12]. The feasibility of using a high-pass to remove DC offsets is also system dependent. A system with a narrow channel and a large amount of signal energy at DC would not be able to incorporate a high-pass filter without destroying the BER to unacceptable levels. On the other hand a system with a wide channel and little energy at DC could tolerate the loss of signal due to a high-pass filter. Razavi in [12] chooses to use a high pass filter to remove unwanted DC offsets in a receiver for IEEE 802.11, (Figure 3-1). To sidestep the problems associated with using nwell material for the needed resistance, Razavi chooses to use the r_o of a MOS device in deep triode. The solution seems to work well for the author but using r_o of a triode device is hard to accurately model and control over process and temperature.

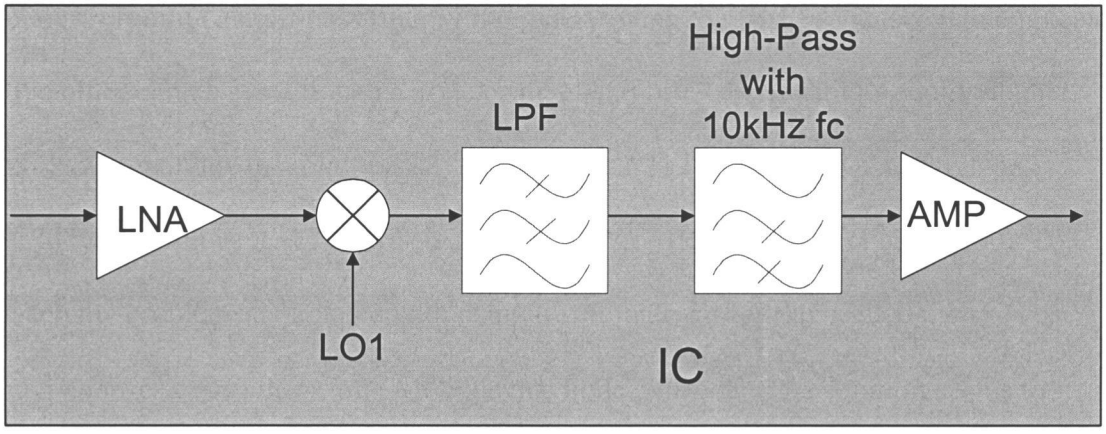

Figure 3-1: Direct conversion architecture used in [12]

In [17] it is argued that a low IF architecture can have the same degree of integration as a direct conversion architecture, with less susceptibility to 1/f noise and DC offsets. As long as the A/D converters have enough dynamic range, the author's claim that the DC offset may be removed with a DSP. Image rejection, channel selection, and demodulation are all carried out in the digital domain with a DSP. To prevent going off-chip to expenses filter components the LNA directly drives the downconversion mixer with no intermediate image filtering. This type of architecture is still very vulnerable to the image problem (only 32dB of image suppression), and still somewhat susceptible to DC offsets, which have been demonstrated to be large enough to saturate stages before the A/D.

In [14] the authors chose a completely integrated superheterodyne low-IF architecture to avoid dc offsets and 1/f noise. A low-IF dual conversion Weaver architecture (Figure 3-2) was chosen due to its high sensitivity, wide dynamic range, and low power consumption. The intermediate frequencies along with the antenna pre-select filter are carefully chosen to adequately suppress the image. Using on-chip polyphase filters the image is suppressed by 60dB. This architecture works well but it is more complex, very susceptible to mismatch, and has higher power dissipation than a direct conversion receiver. Thus, a system implemented in a direct conversion architecture is still desired over a low-IF heterodyne architecture. Noise calculations and results ere not given or discussed except for the total minimum theoretical noise figure, which is a surprisingly low 7.2dB.

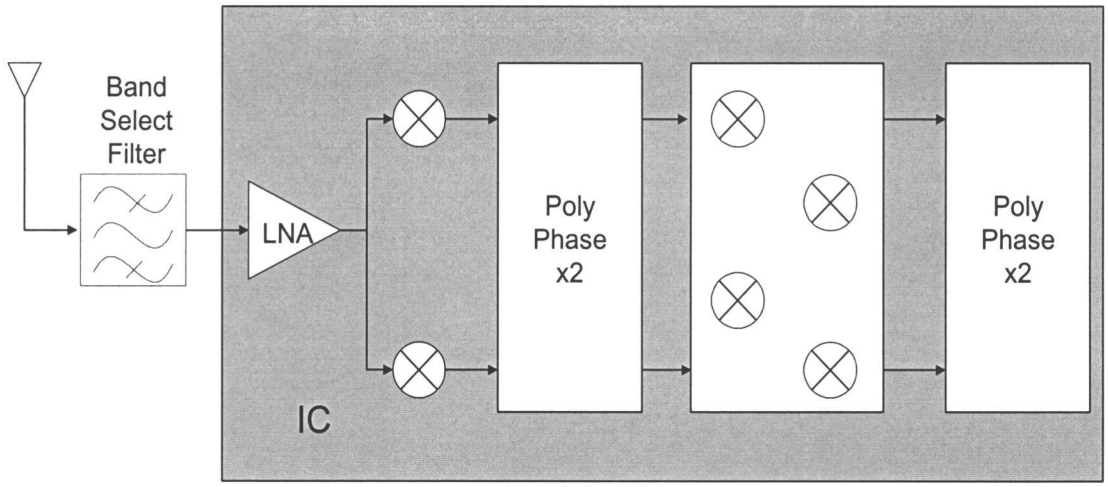

Figure 3-2: Low-IF dual conversion Weaver architecture used in [17]

In [8] two steps were used to convert the RF signal to baseband, called indirect conversion, (Figure 3-3). This is not a true heterodyne or homodyne architecture. The mixer is separated into two mixers but the mixing block may still be viewed as one, so the authors refer to this architecture as indirect conversion. Since mixer flicker noise is directly related to the LO frequency [30] an indirect architecture was used to circumvent the problem. The first mixer converts the signal to a 100MHz IF. The flicker noise from this mixer is high, but the signal will be unaffected since the IF is higher than the 1/f corner frequency. The second mixer converts the IF to DC, but since the LO is at a much lower frequency than a direct downconversion the mixer flicker noise will be lower. No active loads were used in the mixer design, so the only flicker noise contribution is from the switches. This technique improves the cascade NF of the receiver by 5dB. This architecture proposes a solution to the 1/f noise problem but it is

still susceptible to DC offsets and it must rely on the band select filter and LNA to adequately suppress the image.

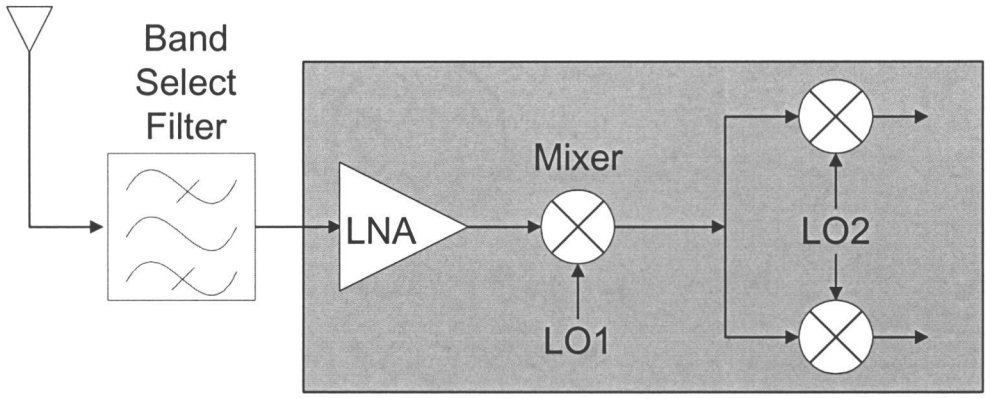

Figure 3-3: Indirect conversion architecture used in [8]

This section discusses different receiver architectures for the implementation of a completely integrated radio. The different architectures are direct conversion, low-IF heterodyne, and indirect conversion. The latter two architectures work well but the direct conversion architecture is still desired due to its simplicity, cost, and power savings if the problems associated with the architecture can be overcome. Table 3-1, shows published results for different low cost, low power receivers. Table 3-2 shows the different individual block topologies of the receiver, offset removal technique, and the process used.

Paper	Gain	NF	Sens.	IIP3	IIP2	1-dB	LO-RF
[8]	61dB	7.4dB	-121dBm	-25dBm	+25dBm		
[9]	58dB	8.6dB	-104dBm	-8.3dBm	+22dBm		
[11]		4.5dB	-104dBm	-21dBm	+22dBm		
[12]	34dB	8.3dB	-80dBm	-9dBm	+22dBm	-21dBm	-47dBm
[14]	20.3dB	7.2dB		-9.5dBm			
[17]	54.5dB	6.2dB	<-100dBm	-6.2dBm			-63dBm
[23]	26-78	14dB	-90dBm	-7dBm		-24dBm	

Table 3-1: Performance of published receivers

Paper	LNA	Mixer	BB Filter	Offset Removal	Process
[7]	CS Cascode w/ ind load	Passive ring Mixer			
[8]	CS Cascode w/ ind load	SBM & Gilbert	4th order Ellip RC		.25u CMOS
[9]	Common Gate	Gilbert w/o tail	2nd- order Butter SCAP 6th Order Cheb SCAP	Feedback loop in limiter Off-chip RC	1u CMOS
10					
[11]	CS	DB w/o tail cur. for headroom	4 Pole Butter followed by 4th order switch Cap	FB loop in SC filter & FF peak det. After BB filter	.6u CMOS
[12]	CS Cascode w/ ind load	SBM w/ R. load	Sallen and Key	On Chip high-pass using a MOS device in triode as Res.	.6u CMOS
[14]	CS Cascode w/ ind load	Mod. Gilbert w/o tail	None, Low-IF		.6u CMOS
[17]	CS Cascode w/ ind load	Cas. current folding	None, Low-IF		.25uCMOS
[18]			Sallen and Key	On chip high-pass, 330pF caps	
[19]				Current DAC in Mixer to modify bias current	BiCMOS
[20]			RC Biquad	Analog FB loop after BB Filt. RC integrator w/ offchip Caps	BiCMOS
[23]	CS Cascode w/ ind load	Gilbert w/ tail cur. & cascode	Sallen and Key anti-alias, 8th ord SC	Current DAC at output of Mixer	.6u CMOS
[37]	CS Cascode w/ R. load	Gilbert w/ tail			.25u CMOS
[38]	CS Cascode w/ ind load				.6u CMOS

Table 3-2: Techniques used in published receivers

3.3 Offset Correction

This section discussed the different techniques used for DC offset cancellation in published receivers. A brief summary of the each cancellation method is given in Table 3-2. Most of the published direct conversion receiver solutions incorporate some

form of offset cancellation. In [4] the authors theorize that one advantage of a CMOS, completely integrated RF IC would be the ability to use a DSP for dynamic correction and control. Yet, only one publication to date has taken advantage of this to dynamically correct for offset.

In one paper the authors do try to eliminate the offset where it occurs in the mixer [19]. The authors explain that the most serious problem of direct conversion is self-mixing of LO feedthrough, and second order distortion. Instead of the commonly used Gilbert Cell architecture, the authors propose an emitter-coupled pair topology in a bipolar technology. The amplitude-modulated waveform is transformed into a pulse-width-modulated signal. Two emitter-coupled pairs are cross-coupled to remove LO products and second order terms. A 3bit DAC is used at the emitter of the bias current device to adjust the bias current to compensate for DC offset and IM2. The results show an IM2 of 37dBm and a DC offset that is below the noise level.

In [12] an on-chip high-pass filter was used to remove any unwanted DC offset. A corner frequency of 10kHz was used, which is about .1% of the chip rate in each I/Q path. Assuming a 10pF capacitor is to be used, the resistance needed to set the pole of the filter is 1.6MΩ. A high-resistance value using n-well material is not practical and would have enormous parasitic capacitance associated with it. Instead, a MOS device in deep triode region was used to achieve the high resistance value needed. This solution seems to work well for the author, but using a MOS device in triode can be difficult to accurately control the resistance across PVT.

The authors in [20] used analog compensation to remove unwanted DC offsets. A feedback network consisting of an active RC integrator is placed after the baseband

LPF to remove offsets. This network is referred to as a servo loop. The technique appears to remove offsets correctly but it does require four off chip capacitors, which adds cost and ruins the implementation of a fully integrated receiver. The authors do not provide any results on how the DC cancellation method responds to dynamic DC offsets. Other analog compensation techniques were reportedly explored but took too long to converge.

In [11] offset correction was performed on-chip with feedback and feedforward loops combined with digital automatic gain control that settles within 160ms. Two feedback integrators are integrated into the baseband filtering to remove offsets and prevent the CM from wandering. Additionally, a switched-capacitor peak detector is used after the baseband filtering to detect the offset level. The offset level is then filtered and subtracted from the baseband filter output and fed to the BFSK demodulator.

The authors in [9] choose to cancel DC offset much later in the receiver chain. Offset cancellation is performed with a DC feedback loop around the limiter after the baseband filtering section. This may be a dangerous solution. A DC offset will experience 38dB of gain before it is cancelled. This technique is acceptable to cancel small static offsets, but in an environment with large dynamic offsets, it could cause the first few stages of the limiter to saturate before the feedback loop. The DC feedback loop measures the average value of the differential limited output, and a differencing stage subtracts this off from the differential input. The loop consists of a RC low-pass filter, with a 40kΩ resistor and a 140uF capacitor, placed off chip. DC feedback is chosen over AC coupling due to the fact that DC feedback components may be placed

outside the signal path. It is stated by the authors, that the 3dB-corner frequency of the loop should be adjusted so that the DC offset is attenuated by at least 20dB compared to the minimum detectable signal. They do not discuss the performance of this loop for dynamic offsets, which will be a serious problem for this type of technique

Offset cancellation is performed on chip with a high-pass filter in [18]. The mixer is followed by a 3rd order Sallen Key elliptic low pass filter. The high-pass has a 150Hz cutoff, using 330pF on chip capacitors. Capacitor this size consume a significant amount of the chip area, and probably do not attenuate the DC offset enough, only 18dB of attenuation was reported. In most processes there is a maximum capacitance area for the chip, which these capacitors would probably consume.

Even though it is a heterodyne receiver, offset cancellation is incorporated in [23]. In a heterodyne architecture the LO is at a different frequency than the RF. This eliminates the problem of LO retransmission that causes time-varying DC. Since the LO and RF are at different frequencies, the retransmitted LO will be filtered out by the band-select filter and narrow-band LNA. Static offset is still present due to LO feedthrough. A six bit DC offset current DAC is used on the output of the mixer to remove offsets. The offset DAC is updated with a baseband DSP.

3.4 CMOS Mixer Design

This section discusses the design of CMOS mixers and their performance. Different mixer structures and their performance are analyzed. In addition, publications that address mixer noise tradeoffs will also be summarized and discussed. Typical

performance for a CMOS Gilbert Cell mixer is a gain of 0-10dB, an IIP3 of 10-20dBM, and a NF of 10-20dB.

In [29] the RF signal is converted to baseband in two steps called quasi-IF by the authors. This technique allows for image rejection. The mixer structure is similar to a conventional Gilbert Cell with the addition of a split PFET load and a cascode bias stage between the RF and LO. The cascode stage is added to increase LO to RF isolation. The authors note that the PFET loads and the RF transconducters dominate the output noise. The circuit was fabricated in a 0.8-um process. The results show typical performance numbers for CMOS Gilbert cell mixers with the exception of a very good LO-RF isolation of –79dB, and a high noise figure of 19dB.

A single balanced structure is used with resistive loads in [12]. Capacitive degeneration at the source of the RF transconductor and inductive loading of the LNA is included to minimize second order distortion. The receiver was fabricated in a 0.6-um CMOS technology. The results for the entire receiver are given but not the results for the individual blocks. The results show a good IP2 of 22dBm, a NF of 8.3dB, a 1-dB point of –21dBm, and LO-RF isolation of -47dB.

In [11], the mixer structure is double-balanced without a tail current source to increase headroom. Biasing for the RF transconductors is done with a replica circuit that is independent of process and temperature variations. A 4-pole Butterworth antialias filter, follows the mixer. Results were only given for entire receiver and not the individual blocks, IIP3 of –21dBm, IIP2 or +22dBm, NF or 4.5dB, and a Sens of –104dBm.

In [9], the mixer is a modified Gilbert cell with no tail current source. PFET loads are biased with the mixer output common mode sampled between two 1K resistors. These resistors also set the desired gain of the mixer. This mixer has a 6dB gain, a 1-dB point of 5dBm, an IIP3 of 15dBm, and a NF of 15dB.

In [23] the architecture used for the 1.9GHz receiver is a image reject heterodyne architecture. The authors use a modified Gilbert cell mixer topology with a tail current and a cascode device between the LO and RF ports. As in [29], the cascode device is added to increase LO-RF isolation. Two load resistors connected between the outputs set the gain and sample the common mode voltage. The output of the CMFB loop is connected to the PFET loads of the mixer. No results are presented for the mixer performance.

In [30] simple equations and design considerations are discussed for flicker and white noise in double-balanced Gilbert cell mixers [30]. Mechanisms for noise in the main contributing devices are discussed with solutions to minimize the effects. Large PFET devices show low flicker noise [28]. They may be used in conjunction with polysilicon resistors, which show no flicker noise, to minimize flicker noise caused by the load. Flicker noise caused by the input transconductor devices can be essentially neglected, because this noise will be upconverted to a high frequency and is easily removed with a low pass filter. Device mismatch will cause a small amount of the input flicker noise to appear at the output. Noise at the input of the switches appears directly at the output, called direct switch noise. At every switching instant a pulse of random width noise appears at the mixer output. This means that that low-frequency noise at the gate of the switch appears at the output without frequency translation. To

minimize these effects and improve SNR, increase the LO transition slope and lower the flicker noise at the switch gate by increasing the size. However, increasing gate area or lowering Vgs degrades mixer bandwidth. From the previous discussing it is implied that flicker noise may be completely removed from the output by increasing the LO transition slope to create a perfect square-wave LO. This is a false assumption because there is also an indirect method by which flicker noise appears at the output. The tail voltage of the switches captures the differential noise of the switching pair. The capacitive current caused by this voltage has a frequency equal to the LO. The flicker noise caused by the indirect mechanism may be reduced by minimizing the capacitance at the source and by applying a LO with sharp transitions. This creates a tradeoff between size and capacitance. White noise from the switches appears at the output when both switches are on. In effect, it acts like a differential amplifier at the instant when both switches are on. This effect puts even more importance on a good, sharp LO signal. White noise created by the input transconductors is converted directly to zero IF with the signal. Simple equations are given to estimate this noise. Results are presented showing consistent results for the equations, noise measurements made with spectre-RF, and measured results from a 0.25-um process.

The circuits in [37] were designed for a superheterdyne architecture, therefore they need a 50Ω match at the mixer input. This is not needed in a direct conversion architecture since no off-chip filtering is required. The authors compare the performance of a double side-band mixer (DSB) and a singe-side band (SSB) mixer. Both mixers use a standard Gilbert cell configuration with a common-gate RF input stage instead of a common-source stage in order to achieve a 50Ω match. The noise

figure of the DSB mixer is expected to be about 3dB lower than the SSB mixer. This aligns closely with the measured results of 12.6dB and 15.9dB. No data is given for linearity.

Table 3-3 summarized the performance results of the different mixer designs discussed in this section. Typically, results for the entire receiver are presented and not for the individual components, therefore, the table has lots of blank spaces.

Paper	Freq.	Process	Gain	IIP3	NF
[9]	900MHz	1-um	6dB	15dBm	15dB
[11]	900MHz	0.6-um			
[12]	2.4GHz	0.6-um			
[23]	1.9GHz	0.6-um			
[29]	1GHz	0.8-um		0.6dBm	19dB
[37]	900MHz	0.25-um		9dBm	12.6dB

Table 3-3: Published mixer results

3.5 LNA Design

This section will discuss different published low noise amplifier (LNA) designs and their performance. Different LNA topologies and their theoretical performance will be expressed in more detail in section 6.2. The LNA is the first device in the receive path after the band select filter. It may be observed from equation 2.2 that the LNA is the most critical device in determining the overall noise performance of the receiver. The LNA output is either directly connected to the gate of the mixer input, or it may be AC-coupled and biased by a large resistor.

Current CMOS LNA architectures and techniques were analyzed by the authors in [38]. All published CMOS LNA publications were compared and analyzed. Currently, four main techniques have been used for CMOS LNA design. The first technique is a simple resistive termination to produce a 50Ω match. The terminating resistor contributes directly to the output noise, which results in a noise figure in the range of 10dB, making this technique unusable. The second technique is $1/g_m$ termination, also known as common-gate architecture. The $1/g_m$ source impedance achieves a 50Ω match. Assuming matched conditions, the minimum noise figure for this architecture is 3dB. Resistive shunt and series feedback is the third type of architecture that has been explored. This technique has shown to have extraordinarily high power dissipation, which makes this architecture unattractive. The fourth and most promising technique is inductive or source(degeneration. This architecture shows the lowest theoretical noise figure but it is a narrow band approach that requires tuning. The authors go through extensive noise analysis and optimization techniques for their amplifier and derive a few fairly simple equations. The actual circuit implemented was a two-stage common-source cascode amplifier with inductive degeneration in a 0.6-um process. The amplifier was designed for 1.5GHz applications and had a NF=3.5dB, Gain=22dB, OIP3=12.7dBm, and an output 1dB compression point of 0 dBm.

The LNA design in [11] is different from most published conventional LNA designs. The input stage consists of two differential pairs in common source configuration with inductive loading. Capacitive cross coupling is added from the gate to the source between the differential pairs to boost gain and give impedance match. A

second stage is cascaded with the first providing additional gain. The two input differential pairs allow for variable gain, either 12 or 28dB. The design was fabricated in a 0.6-um technology but performance for the individual receiver blocks was not presented.

The LNA topology in [12] is a common-source cascode device with inductive loading and degeneration. A 50Ω match is achieved with the inductive degeneration of the input device. The purpose of the cascode device is to enhance bandwidth by killing the effects of C_{gd}, also known as the Miller effect. The load inductor and the capacitive degeneration in the mixer suppress the low-frequency beats generated in the LNA and therefore improve IIP2. No results are given for the amount of improvement. The LNA/mixer combination produces 24dB of gain.

In [9] a common-gate topology was used for the LNA. This type of configuration gives an impedance match with the $1/g_m$ impedance of the input device. This topology is acceptable when a 3dB noise figure can be tolerated. A CMFB loop controls the bias to fix the output bias and allow direct coupling to the mixer. Simulation results show a gain of 20dB, an IIP3 of 12dBm, a 1-dB point of 1dBm, and a NF of 3.4dB.

In [23] a common-source cascode topology with inductive degeneration provides high gain and an impedance match without a physical resistor. The cascode device is added to provide better reverse isolation, and alleviate the effects of C_{gd}, i.e., kill the Miller Effect. An inductive loading was used to increase output impedance and gain. The LNA achieves a NF of 3.5dB in simulation but the actual observed NF is

5dB. The author contributes this difference to the inadequate thermal noise model of short channel MOSFET devices.

The authors in [37] argue that power consumption is a more important factor than cost for the development of RF CMOS. The goal of the authors is to develop RF front-end circuits that meet the specifications for GSM and have comparable power consumption to Bipolar and GaAs technologies. Although the circuits are designed for a superheterodyne architecture their techniques can be used in a direct conversion architecture. A common-source configuration was chosen over a common-gate architecture due to the lower achievable NF. The real part of the input impedance required for a 50Ω match was generated by inductive degeneration. The inductacne required was 1nH, which is approximately the inductance of a bond wire. It is explained that it is beneficial to have the Q of the matching network greater than one. A Q greater than one allows for some voltage gain in the matching network, which can reduce the noise contribution of the input transistor, and reduce the amount of current required in the LNA first stage. This circuit had a Q of 2.5. It was also demonstrated that increased substrate contact can reduce the amount of noise caused by the backgating effect of the resistive substrate under the transistor channel. Increasing the substrate contacts between the fingers reduced the NF by 0.25dB. The drawback of this circuit is that the input match relies on the inductance of a bond wire, which can vary greatly depending on bonding location. No on chip inductors were used, yet a 2dB noise figure was still achieved. This is a much lower noise figure than other published articles with a similar LNA topology, but 18mA of current was consumed to do so, which conflicts

with the author's goal of low power consumption. Most other published designs consume approximately 3-6mA.

In [7] a cascode common-source architecture was used with inductive degeneration. A LC tank is used to modify the transfer function of the LNA to help filter out the image frequency. The inductor also helps minimize the NF by nullifying the parasitic capacitance from the cascode stage. Only one stage is used with 18dB gain, resulting in a mediocre 4.8dB noise figure.

Table 3-4 summarizes the performance of the different LNAs discussed in this section. It may be concluded from these papers that the common-source architecture has the best noise performance but it is harder to implement than a common-gate architecture, which has a higher noise figure.

Paper	Freq	Process	Gain	NF	IIP3
[7]	5 GHz	0.25-um	18dB	4.8dB	
[8]	900 MHz	0.25-um	25dB	3.3dB	15dBm
[9]	900 MHz	1-um	20dB	3.4dB	12dBm
[11]	900 MHz	0.6-um	12-28dB		
[14]	2.4 GHz	0.6-um		1.8dB	2dBm
[17]	1.8 GHz	0.25-um		2.2dB	
[37]	900 MHz	0.25-um	14dB	2dB	-2dBm
[38]	1.5 GHz	0.6-um	22dB	3.5dB	

Table 3-4: Published LNA results

4.0 DIRECT CONVERSION OFFSET CORRECTION MIXER

4.1 Introduction

As discussed earlier, direct conversion requires some form of offset correction. Recently, a few solutions have been published, but most of them require off chip components or wait many stages past the mixer to remove the offset [9] [10] [11] [12] [13] [20] [21]. The focus of this research has been to design a system to correct for the offset where it occurs in the mixer. This will make the design of downstream stages easier and will prevent the offset from being amplified. To maintain the attractiveness of the direct conversion architecture the solution needs to be completely integrated, requiring no off chip components. All circuit design is done in 0.35-um CMOS but the approach could easily be implemented in a BiCMOS or SOI-CMOS process.

The main advantage of RF CMOS is the ability to integrate digital signal processors or DSP [4]. To take advantage of this ability, the solution for removing offsets in a direct conversion mixer is shown in Figure 4-1. The DSP comprises of a dual-loop algorithm to track the static and dynamic nature of the offset [43]. The A/D is used to measure the offset and the DSP controls the D/A to adjust the mixer load current to compensate for the offset current. Before more detail is given on the proposed solution, it is helpful to review CMOS mixer basics and how offsets arise.

Professor John Stonick of OSU first proposed the system level solution shown in Figure 4-1. A number of students have contributed to this research. Christian Holenstein made contributions to the DSP correction algorithm [43]. Mark Lehne

contributed the initial mixer and DAC designs. My contribution has been the mixer and DAC redesign, implementation, and testing. The mixer presented in this thesis is the same topology as proposed by Mark, but in a different process with a few modifications. Changes in circuitry were required due to the change of process. The DAC presented in this thesis is similar to Mark's but not the same. The DAC required a complete redesign in order to be implemented. Additionally, Matt Coe made contributions on the implementation of the DSP correction algorithm and on the PCB design for the system.

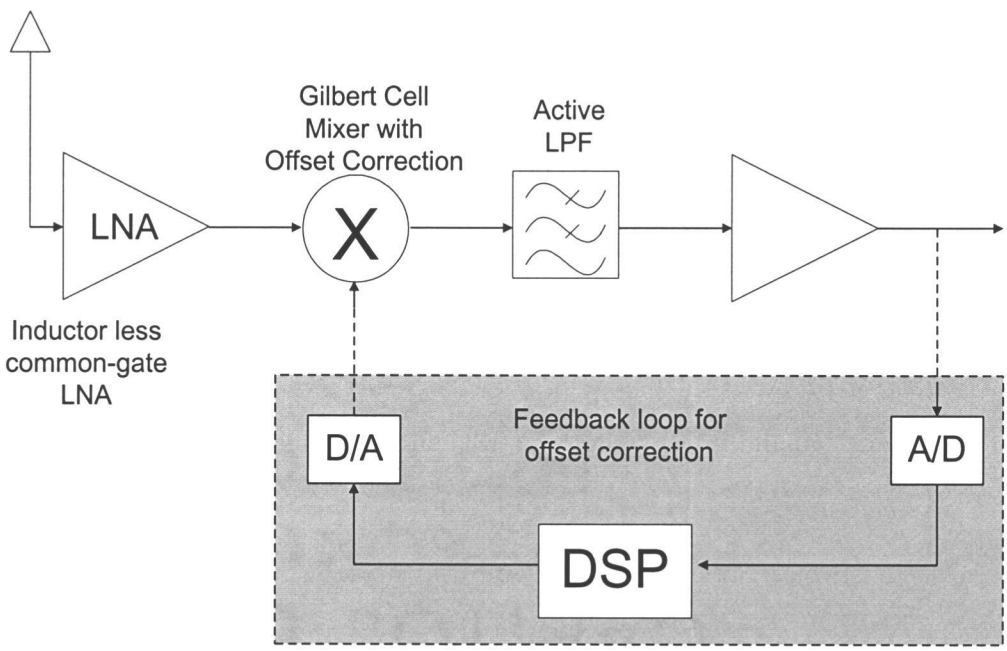

Figure 4-1: System level solution for DC offset correction

4.2 CMOS Mixer Basics

Most CMOS mixers are versions of a mixer first proposed by Barrie Gilbert, and are appropriately named Gilbert cell mixers [44]. The incoming RF voltage is converted into a current, multiplied by the LO in the current domain, and then converted back to a voltage at the output. The simplest form of this form of this type of mixer is the single balanced mixer sketched in Figure 4-2. These types of mixers have many advantages over other types of mixers (i.e. diode mixers, square-law mixers, and passive mixers). Gilbert cell type mixers may be designed with gain, which is desirable in order to improve system performance. RF to LO isolation is much better, so offsets caused from self-mixing will be less in a Gilbert cell architecture. They also have better linearity over architectures that rely on circuit nonlinearities to perform frequency conversion.

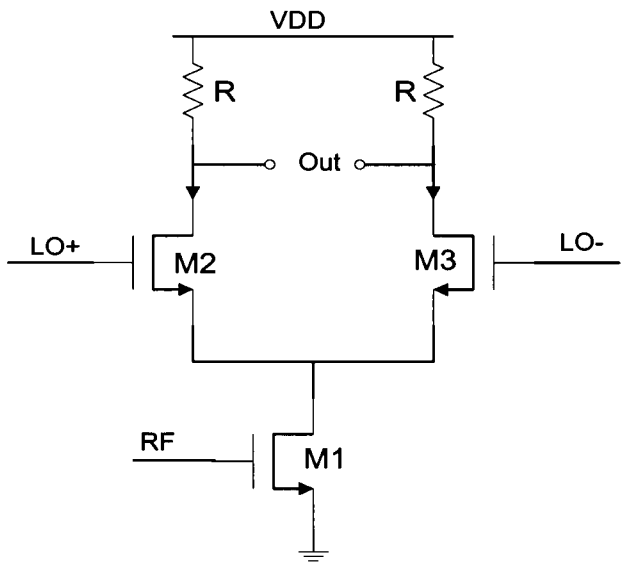

Figure 4-2: Single balanced mixer

In Figure 4-2, the RF waveform is converted to a current by the input transconducter, M1. The local oscillator (LO) waveform is chosen large enough to completely turn off one of the LO switches (M2 & M3) forcing the current to alternate from one switch to the other at the LO frequency. Analytically, this can be viewed as multiplying the bias and RF current by a square wave ($sign[\cos(\omega_{LOt})]$) [1]:

$$i_{out} = sign[\cos(\omega_{LO}t)][I_{bias} + I_{RF}\cos(\omega_{RF}t)] \quad (4.1)$$

$$sign[\cos(\omega_{LO}t)] = \frac{4}{\pi}\cos(\omega_{LO}t) - \frac{4}{3\pi}\cos(3\omega_{LO}t) + ... \quad (4.2)$$

At the circuit output the current is converted back to a voltage by the resistive load. The products of two sinusoidal waveforms multiplied together are the sum and difference components of their frequencies. The output consists of these components at odd harmonics of the LO due to the square wave, see equation 4.2. In addition, the fundamental LO will appear directly at the output due to the multiplication of $I_{Bias} * sign[(\cos\omega_{LO}t)]$. To prevent the LO from appearing at the output two single balanced mixers may be connected to form a double balanced mixer. The single-balanced mixers are connected in antiparallel, (see Figure 4-3). This cancels the LO terms, and doubles the RF signal at the output. The gain of these types of mixers is:

$$A_v = \frac{2}{\pi} g_m R_{out} \quad (4.3)$$

where g_m is the transconductance of the input device, M1 or M2, and Rout is the output impedance of the mixer, R in Figure 4-3. The $2/\pi$ term comes from the fundamental

component of a square wave ($4/\pi$) divided by 2 from the frequency translation ($\omega_{RF} - \omega_{LO}$).

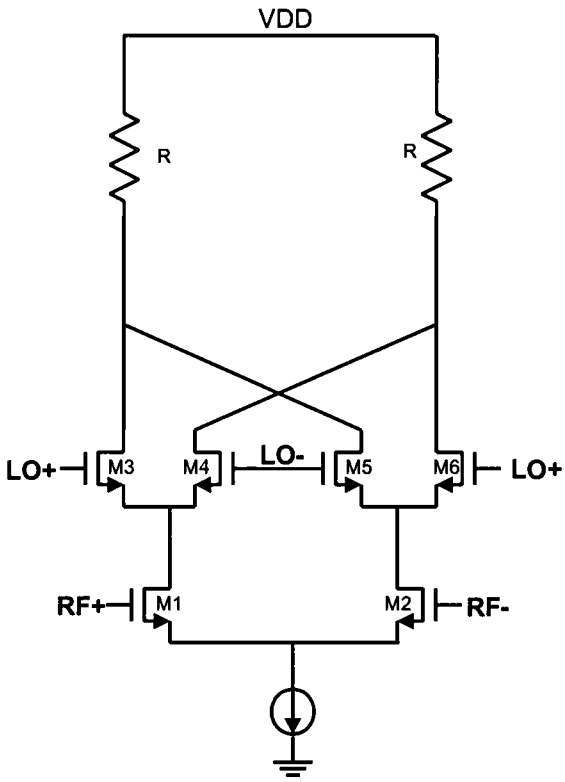

Figure 4-3: Double-balanced mixer

4.3 Characterizing the DC Offset

This section discusses in more detail how offsets arise and the different types of offsets in a mixer.

LO leakage through the substrate will cause some of the LO signal to appear at the RF input. In equation 4.4, the A_l signal is the LO leaked into the RF input port. This signal is then converted to a current by the input transconductor, M1 or M2. The LO leakage current is then mixed with the LO square from the switches, creating a DC term

and a double frequency term, as shown in equation 4.4. The LO signal is shown as a sine wave in equation 4.4 for simplicity. It is actually a square wave, see equation 4.2.

$$(A_I \cos(\omega_{LO} t))(A\cos(\omega_{LO} t)) = \frac{AA_I}{2} + \frac{AA_I}{2}\cos(2\omega_{LO} t) \quad (4.4)$$

The DC energy manifests itself as a differential DC offset current at the output, as shown in Figure 4.4. This differential offset current is then converted to a DC offset voltage by the output load.

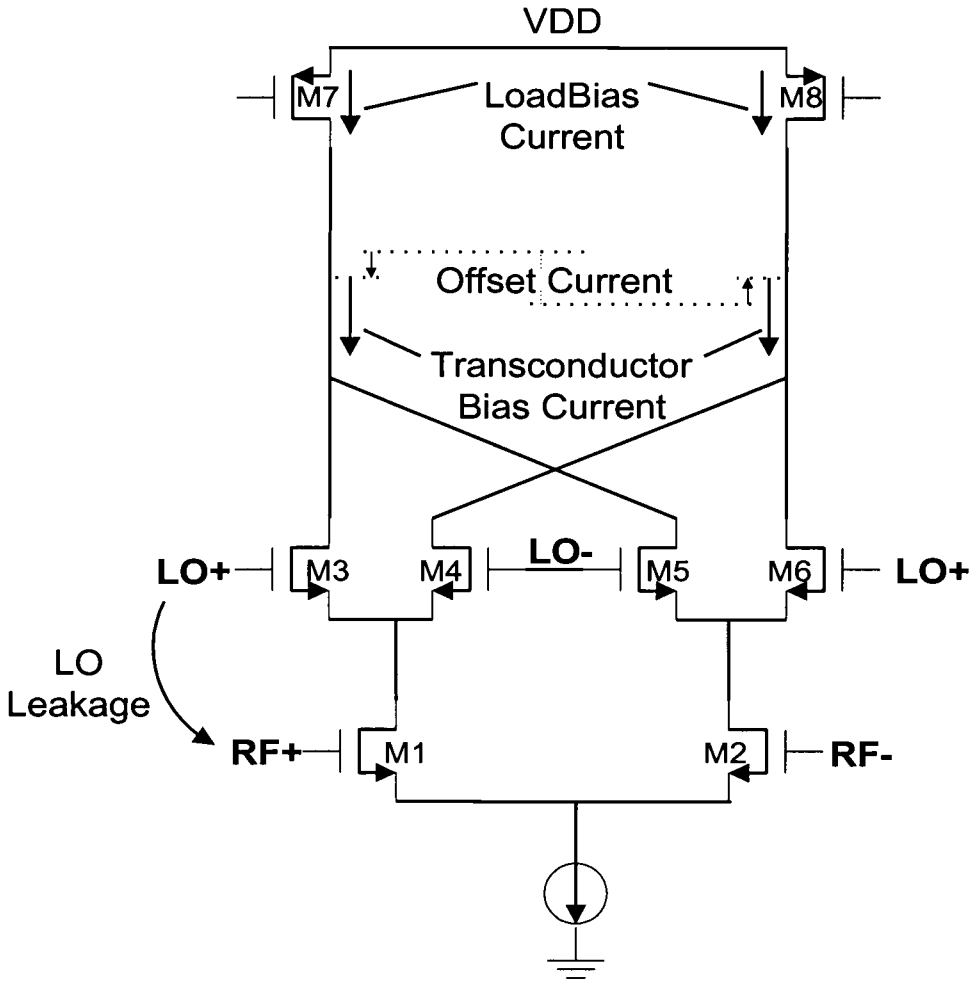

Figure 4-4: DC offset currents

It is important to differentiate between a common- mode and a differential offset. The top plot of Figure 4-5 demonstrates a common-mode offset. The differential signals shift away from the desired CM voltage. This type of offset may be compensated for with a common-mode feedback circuit (CMFB). The lower plot of Figure 4-5 shows a differential offset. The differential signals will shift away from each other. It is important to notice that the CM voltage will be unaffected by this type of offset, therefore, a CMFB circuit will have not affect on this type of offset.

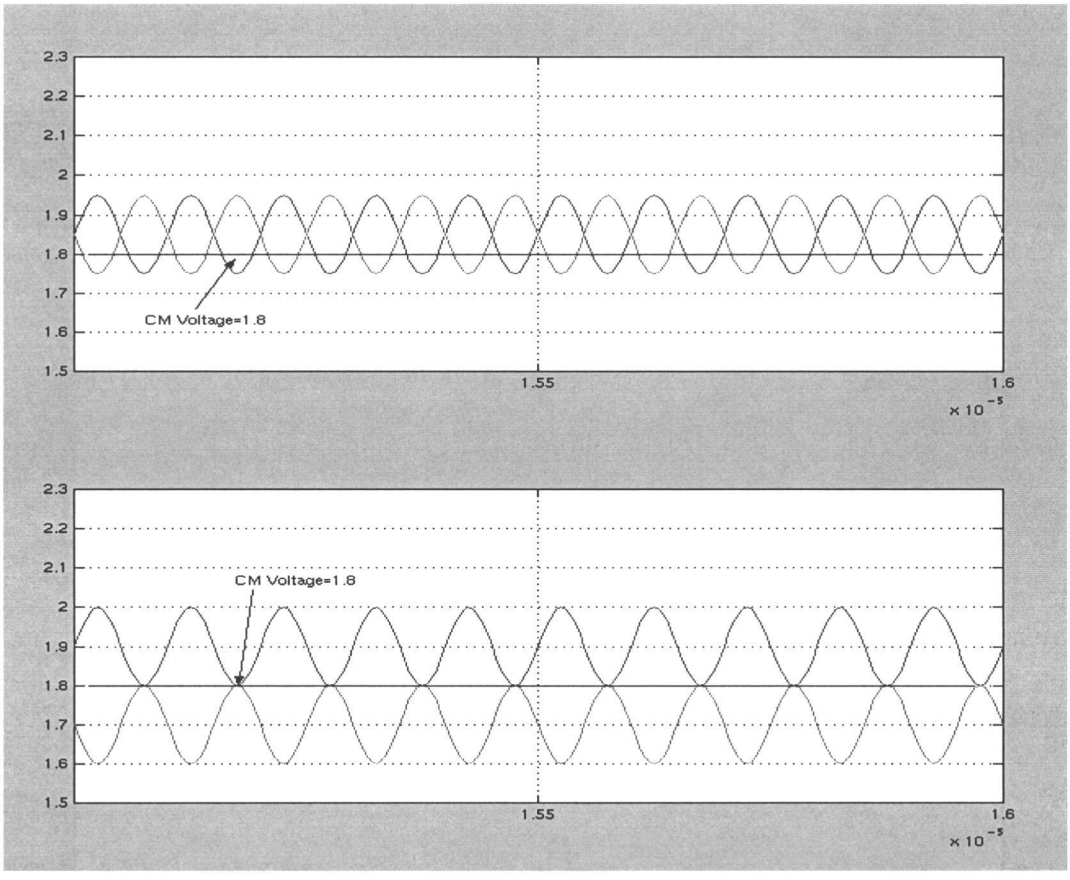

Figure 4-5: Common-mode offset (top) vs. differential offset (bottom)

In this research a CMFB circuit will correct for any CM offset, while the DSP algorithm controlling the DAC to adjust the load bias current will correct for differential offsets (Figure 4-1).

4.4 Compensating for Offsets

The goal of this research is to design a mixer that has loads that may be controlled by a DSP algorithm through the DAC, as seen in Figure 4-1. In Figure 4-6, the offset current caused by self-mixing is nullified by adaptively adjusting the load current in the PMOS loads (M6 and M7) of the mixer to inject a differential cancellation current.

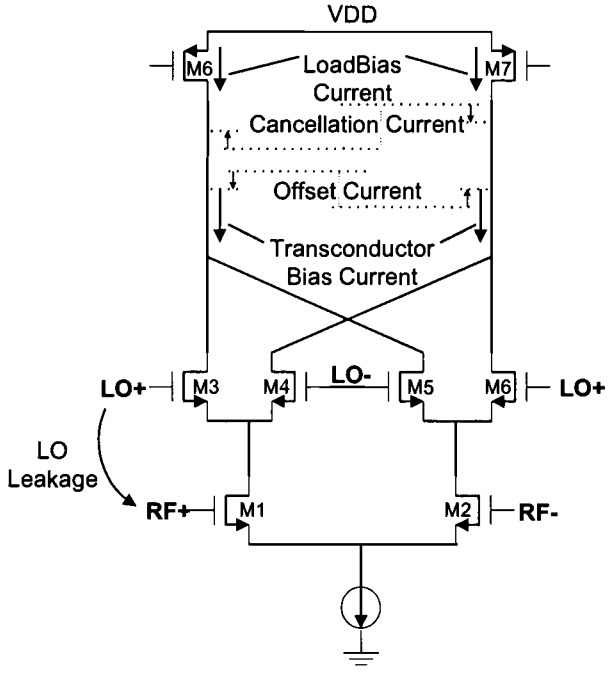

Figure 4-6: Canceling the DC offset

In the case of a dynamic offset, there will be some inherent time delay for the offset to be measured and compensated for by the feedback loop. During this delay the DC offset will degrade the SNR of the system, so the delay should be minimized.

4.5 Mixer Design

The mixer schematic is shown in Figure 4-7. The mixer tail current is controlled by a simple current mirror through M1. A tail current of 2.5mA is chosen to give the approximate g_m value desired (~3-4mS) for the input transconductors and maintain the goal of low power consumption. The RF input transconductors, M2 and M3, are chosen to be 30/0.4 to increase the current density for improved IIP2 and IIP3. The LO switches, M4-M7, are chosen to be 80/0.4 again for increased current density but with a slightly larger size than the input transconductors for better flicker noise performance. Flicker noise from switches appears directly at the output and can degrade noise figure [30]. Two 1.2K poly resistors are connected between the output legs for two reasons: one, to sample the common-mode voltage, and two, to set the output impedance, R_{out}. Shunt capacitors are placed at the output to create a LPF with the 1.2K resistors. The single-pole RC filter removes LO/RF feedthrough and has a 260MHz cutoff. The top PFET loads, M8-M11, are made large to minimize their flicker noise contribution directly to the output. The PFET loads are split in two, as shown in Figure 4-7 by M8 and M9, or M10 and M11. One provides three-fourths of the bias current needed, M9 or M11, while the other, M8 or M10, provides one-fourth of the bias current that will be dynamically changed to correct for offset voltages. Splitting the load will give better

noise performance than a single load controlled by the DAC. The DAC is much noisier than a simple current mirror to bias the load PFET. Additionally, the DAC does not need full control of the PFET bias current because the offset current will never be as large as the bias current. Typical mixers exhibit ~ –30dB of isolation between the LO and RF input ports. Assuming this isolation and a 0dBm LO square wave, the offset current will be approximately 25uA, which is only a small percentage of the bias current. The CMFB loop is connected to the bottom current mirror. A 10pF capacitor in series with a 1k resistor is needed to compensate the CMFB loop and produce a phase margin greater than 45°.

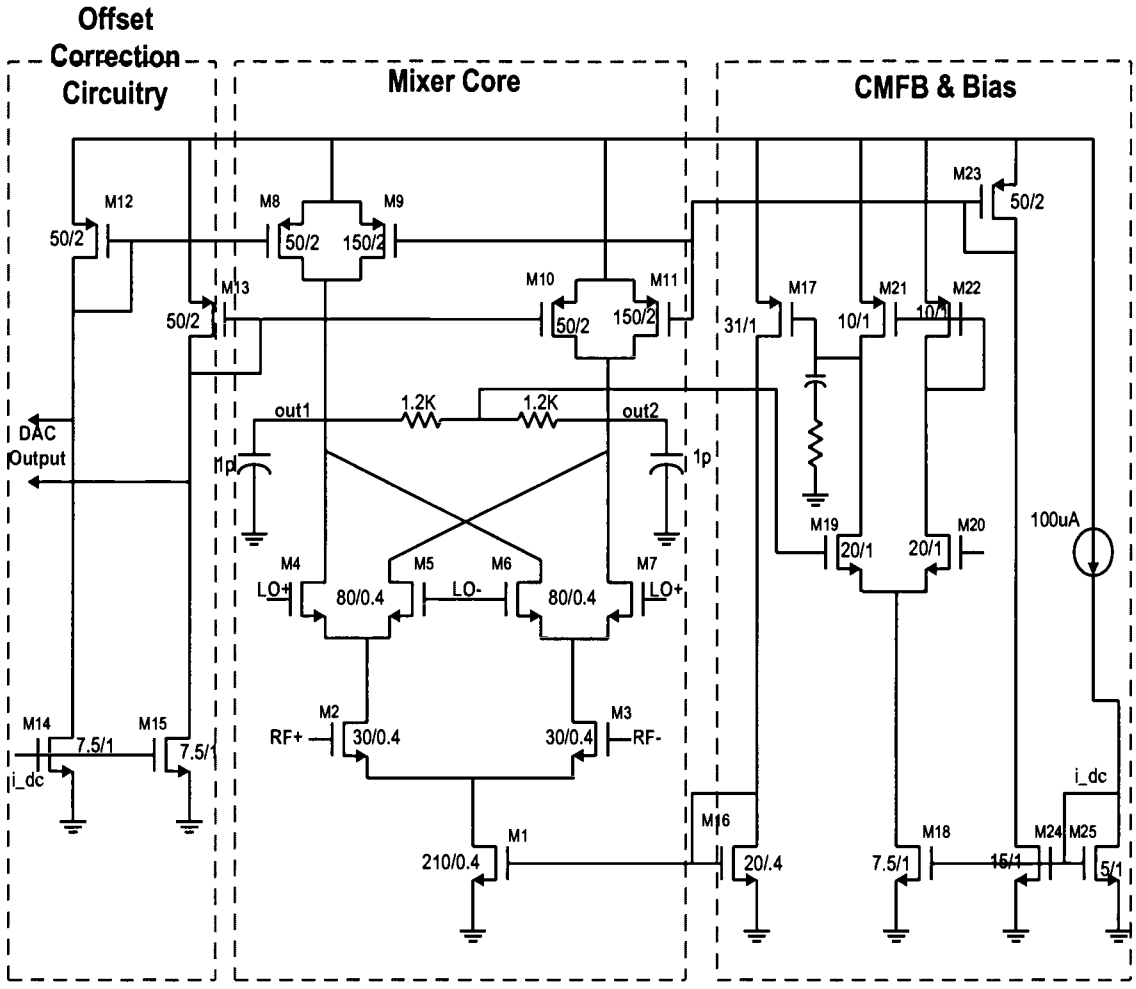

Figure 4-7: Direct conversion mixer schematic

4.6 DAC Design

The purpose of the DAC is to interface between the DSP and the mixer. The DAC is controlled by the DSP to dynamically adjust the PMOS load current in the mixer, see Figure 4-1. The DAC design is a six-bit current-steering device, (see Figure 4-8). The DAC has a full-scale range of 315uA. In order to be able to steer the current differentially the DAC supplies one-half of the bias current needed for M33 and M34 in

Figure 4-8, or M12 and M13 in Figure 4-7. M7 and M8 (Figure 4-8) supply the other half of the bias current. Under ideal conditions with no offsets present in the mixer the DAC input would be set to 100000 in order to supply half the bias current needed for M33 and M34. Therefore, the actual correction range for the DAC is half of the full scale range. Each bit is proportionally mirrored off the bias current of the mixer, M25 in Figure 4-7. The LSB for the DAC is set at 5uA, therefore the MSB is 160uA. In an actual system, 160uA of offset cancellation would probably never be needed but for a test chip extra range was included to characterize the device. Simple inverters, M21-M32 are used to control the differential pairs that steer the current to the mixer legs.

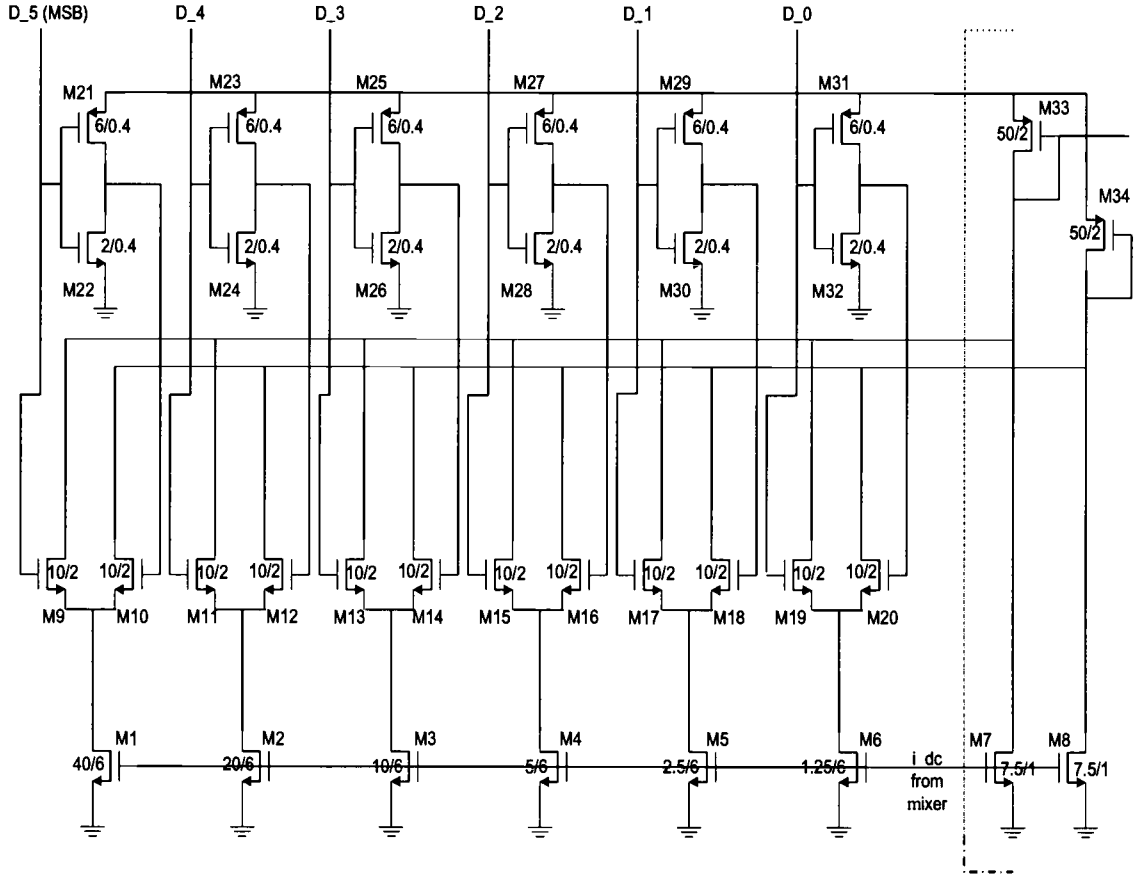

Figure 4-8: Current DAC design

In order to use this type of simple, current mirroring DAC, the offset must be linear. Figure 4-9 shows simulated induced offset voltage created in the mixer and the offset current needed to remove the offset. As can be seen from Figure 4-9, the offset is very linear.

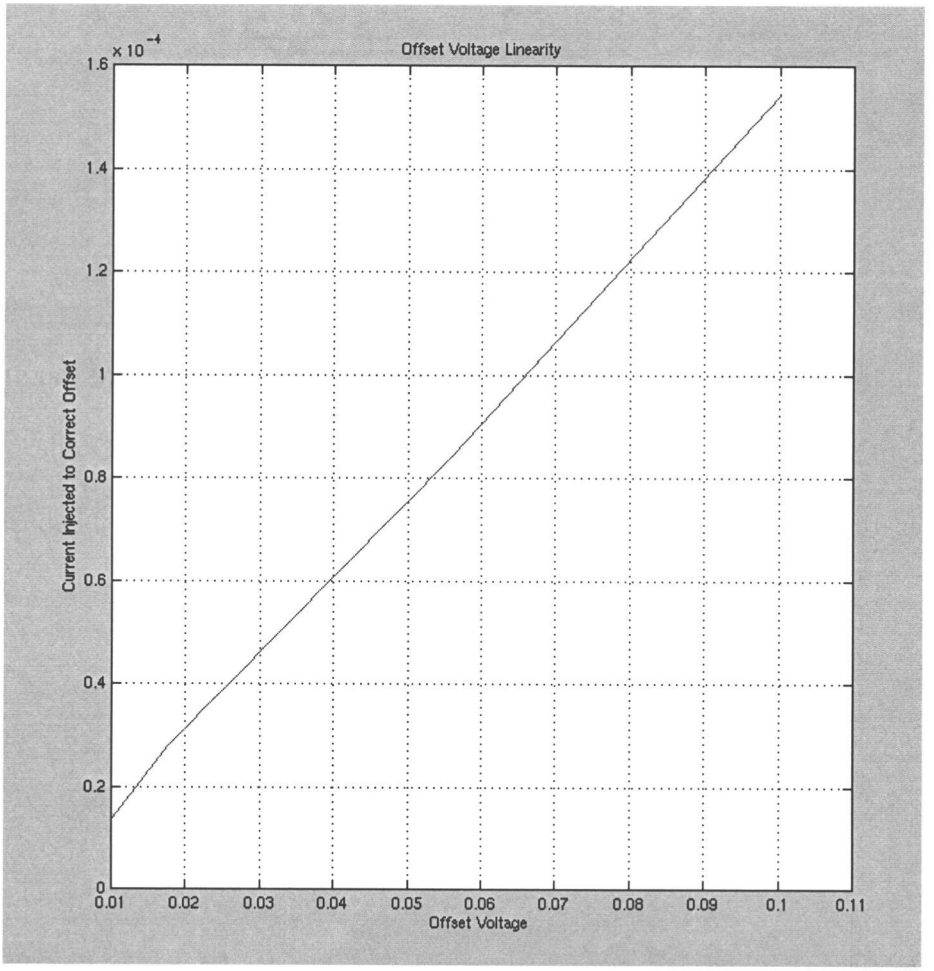

Figure 4-9: Offset linearity

4.7 Mixer Layout

The mixer is layed out using a 0.35 TSMC CMOS process. The mixer layout is critical to its performance, especially at high frequency. As mentioned earlier, any mismatch between devices creates DC offset and second-order distortion problems. Also, LO to RF isolation must be considered, as well as capacitive coupling between metal layers. The input transconductors are the most critical devices in the circuit. Since the transconductors are small, they were not interleaved. They are kept close together so the gradient over the devices will be approximately the same. The capacitive coupling caused by interleaving would be more harmful than the improvement in matching. One um/mA is used as the minimum width for metal traces to prevent electromigration, the narrowing of line widths over a period of time from large currents through a line that is too small. The two sides of the mixer are designed to be as symmetric as possible. This gives two advantages. The first is device matching, and the second is that all metal traces have the same length/width ratio and therefore the same resistance and capacitance. Substrate ties should be placed liberally and as close to every transistor as possible to prevent substrate noise. The LO and RF traces should be kept orthogonal and far apart to provide isolation. The mixer core layout is shown below in Figure 4-10.

A buffer amplifier is added to the fabricated mixer design to shift the desired RF input range to the proper range required for the selected A/D converter. This circuit amplifies the DC offset, but as long as the correction algorithm is working correctly the offset should still be compensated for. The goal of future research is to eventually

implement the DSP correction algorithm on chip with the mixer. The DSP noise and clocking will have some effect on the performance of the mixer. To simulate this, a string of D-Flip Flops were added to the layout to create digital noise. Each block in the layout was heavily guard-banded and placed on separate power supplies in order to reduce its effects on other blocks. The final layout is shown in Figure 4-11.

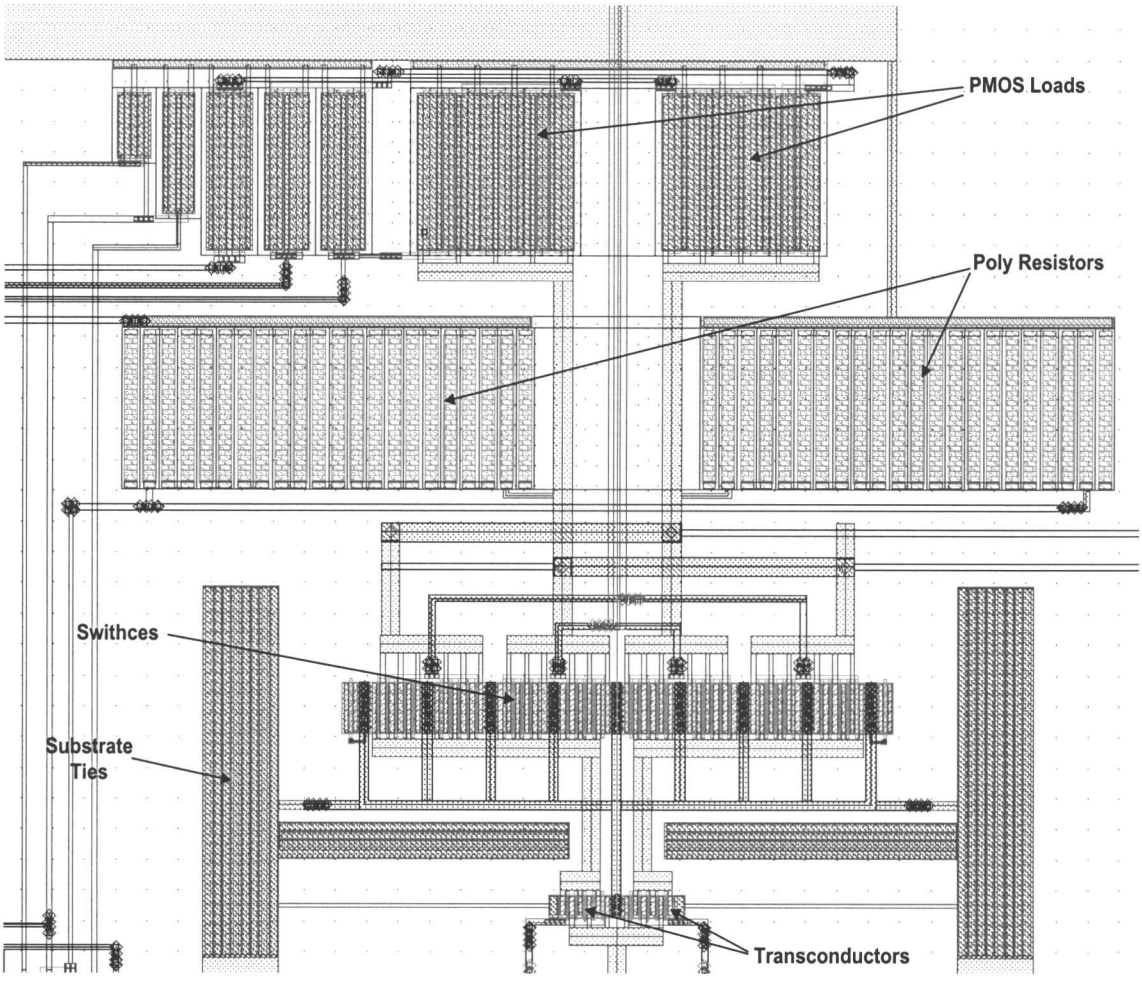

Figure 4-10: Mixer core layout

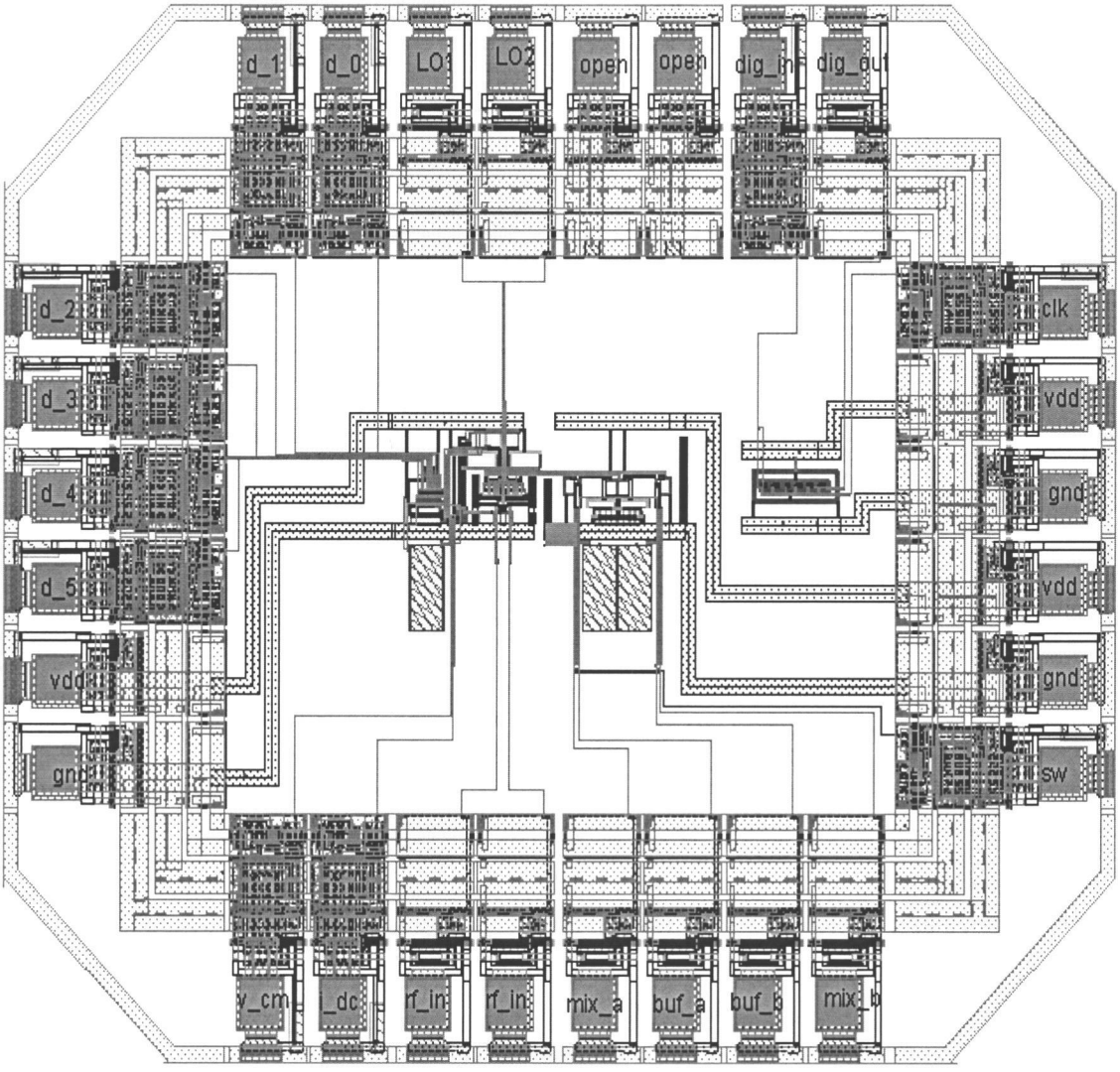

Figure 4-11: Complete mixer layout

5.0 MIXER RESULTS

5.1 Simulation Results

The mixer is designed to have a gain of 8dB, a NF less than 18dB, and 1-dB point greater than 0dBm. A mixer that meets these specifications could be incorporated into almost any system for Bluetooth, HomeRF, or WLAN. The mixer results are summarized in Table 5-1. Figure 5-1 shows the IIP3 result from Cadence SpectreRF SPSS analysis.

Gain	8dB
IIP3	17.6dBm
1dB	6.5dBm
Noise Figure	14.5dB

Table 5-1: Mixer simulation results

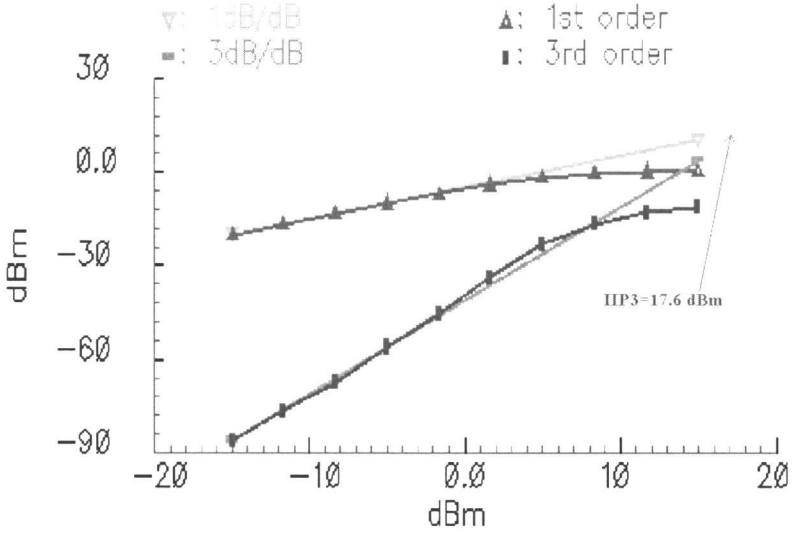

Figure 5-1: Cadence SpectreRF IIP3 result

In the past simulators such as spice could not accurately measure the noise performance of mixers due to the switches, and the frequency translation of noise due to circuit nonlinearities. More recent simulators such as SpectreRF can more accurately predict mixer noise performance. In design situations like this, it is important to verify theoretical and simulated noise analysis. The authors in [30], [26], and [28] all try to characterize and create simple models to predict the noise performance of CMOS Gilbert Cell type mixers. The techniques in [30] seem to create the most usable and accurate model. As discussed earlier and in [30] it is important to recognize that low frequency noise (1/f noise) from the transconductance FET's does not affect the output signal because the low frequency noise is translated to the LO frequency. Another important factor is that flicker noise associated with the switches is directly related to the LO frequency and indirectly related to the slope (transition time) of the LO. A 0dBm LO is chosen because it is a typical value for on chip LO amplitude. This paper confirms that better noise performance may be achieved by increasing the LO amplitude, but in [16], [28] they point out that over driving the transistors too far into the triode region will degrade linearity performance. In [30], after analyzing the mixer noise sources a simple equation is given to predict the output noise:

$$Vo_n^2 = 8kTR_L(1+\gamma(\frac{2R_L I}{\pi A}) + \gamma g_m R_L \quad (5\text{-}1)$$

where, I is the tail current through each side (1.25mA), A is the LO amplitude (0.316 V), R_L is the resistive load (1.2K), and g_m is the transconductance of M2 or M3 in Figure 4-7. The second term in equation 5.1 is the noise contribution from the switches and the last term is the white noise contribution from the transconductors. This equation predicts the output noise voltage to be 11nV/sqrt(Hz), NF=13.7dB. Analysis

from PSS analysis in SpectreRF predicts the output noise voltage to be 13nV/sqrt(Hz). The mixer noise figure could easily be three to four dB higher due to flicker noise. Accurate models for flicker noise were not available at the time of design for the TSMC 0.35u process.

To simulate offsets caused from LO feedthrough, –10dBC of LO is coupled into the RF port. Figure 5-2 shows the mixer operation with and without using the DAC for offset correction.

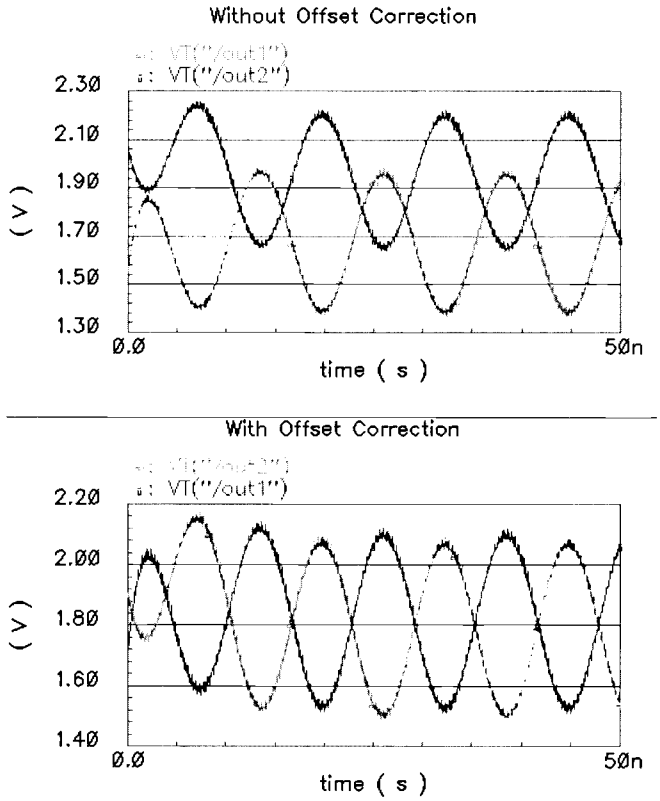

Figure 5-2: Mixer operation with offsets

This work shows that the DC offset problem can be corrected for in the mixer by controlling the bias of the loads. This solution requires no off-chip components and

makes the direct conversion architecture feasible for low cost, low power wireless transceivers.

5.2 Test Results

The mixer was fabricated in a TSMC 0.35-um process and packaged in ASAT's 28 pin PSOIC. The mixer test board incorporated the mixer, baluns, bias-T's, A/D converters, and a FPGA implementing a dual-loop algorithm to measure the offset. Figures 5-3 and 5-4 show the test setup. The mixer does not work as designed, due to mistakes made with pad circuitry. The mixer output has no response to changes in bias voltages or to the DAC inputs. The cause for this was initially though to be incorrect bonding or die orientation. After failed attempts to etch through the top of the package, the package was grinned off. The die orientation was correct and the bonding assumed to be correct since the die was correctly placed. After close inspection it was noticed that the bias current input (I_dc, M25 in Figure 4-7) is connected to a digital pad (wpadin), which includes a large buffer. Therefore, the mixer will never receive the correct bias current. It was unsuccessfully attempted to bypass this pad with a probe station. Considerable time was spent on the RF pads, but the current bias pad was overlooked. In addition to the mixer output not responding the buffer power supply, ground, and the gate of pass transistors at the mixer output will short together after some variable time of being powered up. Currently, there is no definite explanation for this problem but it is suspected that it is also pad related. The pad is the only location where these three traces come together and cross. The pad used for the gate of the pass transistors is also wpadin.

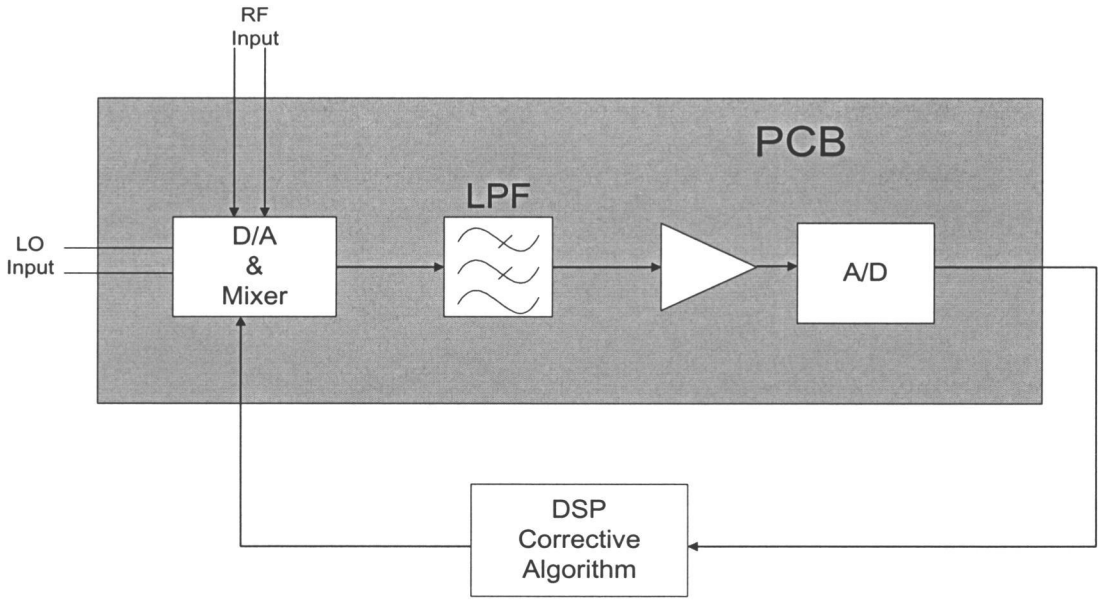

Figure 5-3: Prototype design

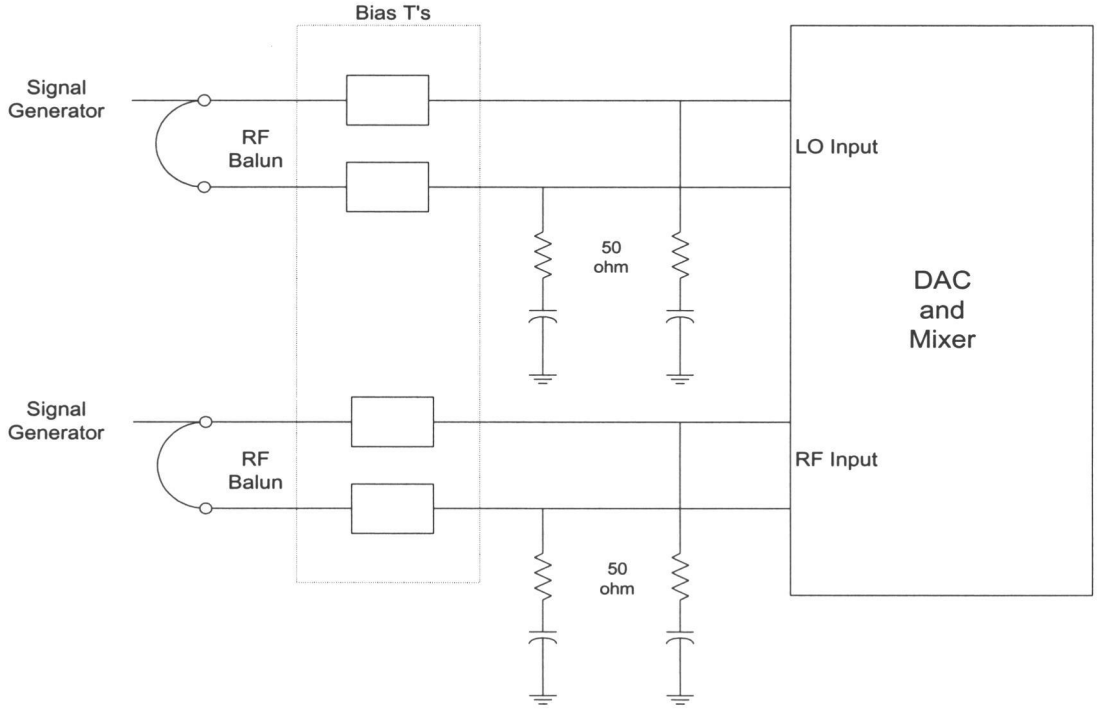

Figure 5-4: RF/LO biasing for prototype design

6.0 SAMPLE SYSTEM FOR DIRECT CONVERSION MIXER

6.1 Introduction

The direct conversion architecture is attractive for home networking applications due to its lower cost, low power, and the fact that it can be completely integrated. Some experts argue that direct conversion is not a viable solution for Bluetooth because of the large amount of signal that would be present at DC due to the protocol. This section will present an all CMOS RF Front End that will meet Bluetooth specifications assuming a spectrally efficient protocol.

Carrier Frequency	2.4-2.483 GHz
Modulation	1Mb/s GFSK
Operating Range	0-50 meters
RX Sensitivity	-70dBm
1-dB Point	-20dBm
IIP3 Point	-16dBm

Table 6-1: Key Bluetooth specifications

6.2 LNA Design

This section discusses different types of CMOS LNA designs and their theoretical performance. In addition, two LNA designs are presented that could be incorporated with the mixer to meet Bluetooth specifications.

Designing good LNAs is difficult in a standard CMOS process. MOS devices are noisier than their bipolar counterparts and it is difficult to build good passives in

standard CMOS. There are two possible architectures for building LNAs with a suitable NF in CMOS: common-source configuration with inductive degeneration, and a common-gate configuration [38].

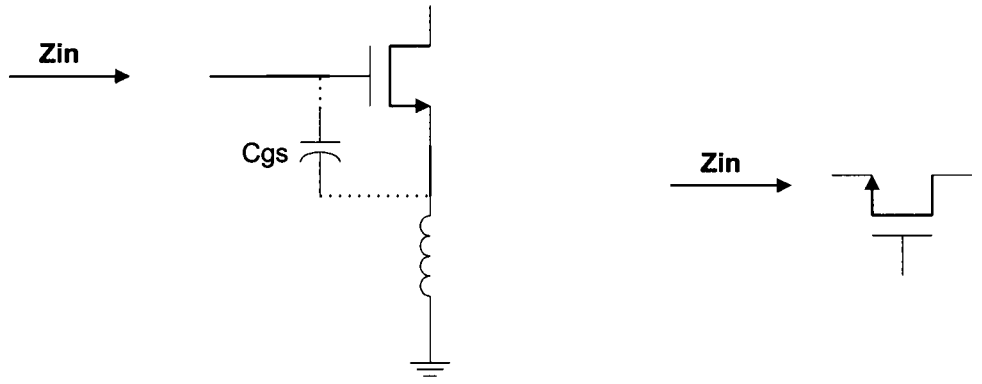

Figure 6-1: CMOS LNA architectures

The common-source architecture uses an inductor at the source to create a real impedance that can be matched to the input impedance, commonly 50Ω, (see Figure 6-1a). From the small signal model, including C_{gs}, the input impedance for an inductively degenerated device is:

$$Zin = \frac{1}{sCgs} + sL + \frac{gmL}{Cgs} \quad (6.1)$$

From the equation it may be observed that the last term in the equation is a real impedance. The value of inductance needed in the source is typically in the 1-3nH range. Typical bond wires have inductances in this range and provide reasonably high Q values. With this type of architecture, no noise is introduced from the matching

network and no on-chip inductors are needed if a bond wire is used for the source inductor. An additional off-chip inductor is usually needed in series with the gate to select the resonant frequency of operation. This is a narrow-band approach since the impedance is only real over a small frequency range. The matching network improves the noise performance of this type of architecture. The Q of the matching network amplifies the input signal before reaching the noisy active device. For convenience the Q is listed below.

$$Q = \frac{\omega_o L}{R} = \frac{\omega_o (Ls + Lg)}{Rs + \frac{g_m Ls}{C_{gs}}} = \frac{\omega_o (Ls + Lg)}{2Rs} \quad (6.2)$$

The theoretical minimum Noise Factor for this type of architecture is [1]:

$$F_{\min} = 1 + 2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_T}\right] \quad (6.3)$$

where α is gm/gdo (one neglecting short channel effects), and γ is the coefficient of channel thermal noise (two-thirds neglecting hot electron effects). The problem with this type of architecture is its sensitivity to device variations and package parasitics. Incorrectly modeled components or variations could significantly change the input impedance match.

In a common-gate architecture the $1/g_m$ input impedance of the source is used to create a 50Ω match. It has a higher theoretical minimum noise figure due to the drain to source resistance. This type of architecture is not as sensitive to device parasitics so it is easier to implement than a common-source architecture with inductive degeneration. The ease of implementation comes at the cost of a higher noise figure. The theoretical minimum noise figure is [1] [38]:

$$F = 1 + \frac{\gamma}{\alpha} \quad (6.4)$$

The minimum noise figure is 2.2 dB if short channel effects and excess thermal noise due to hot electrons are neglected. In practice, considering these effects, the minimum theoretical noise figure is around 3dB.

The sensitivity requirement for Bluetooth (-70dBm) allows for a higher than normal NF in the LNA, approximately 5dB. A common-gate architecture is chosen due to its ease of implementation, and lower susceptibility to parasitics. The LNA in Figure 6-2 is a fully differential design. The $1/g_m$ impedance of M3 and M4 provide the real impedance value required for impedance match. The desired frequency response could not be achieved with $1/g_m$ set to exactly 50Ω. The input impedance of M3/M4 is set to a higher value, 150Ω, and then an off-chip matching network is used to match this impedance to 50Ω. The matching network includes the package parasitics: pad capacitance, and bond wire inductance. A simple current mirror biases the gates of M1 and M2. The current through each side of the circuit is 2.5mA. The gates of M3 and M4 are biased at 2V by the 5K resistor and current mirror. A resistive load is used to prevent the use of on-chip inductors. Some systems may require a lower noise figure and higher gain in the LNA. In that case the resistive load would need to be replaced with an on-chip inductor. The inductor could also be implemented as a combination of bond wire and on-chip inductor or bond-wire and off-chip inductor. The LNA simulation results are shown in Table 6-2. Figure 6-3 shows the 1-dB compression point simulation from SpectreRF. Figure 6-4 shows the NF measurement from PSS analysis

in SpectreRF, and Figure 6-5 shows S11 from SP analysis in SpectreRF. All LNA simulations were performed with SpectreRF.

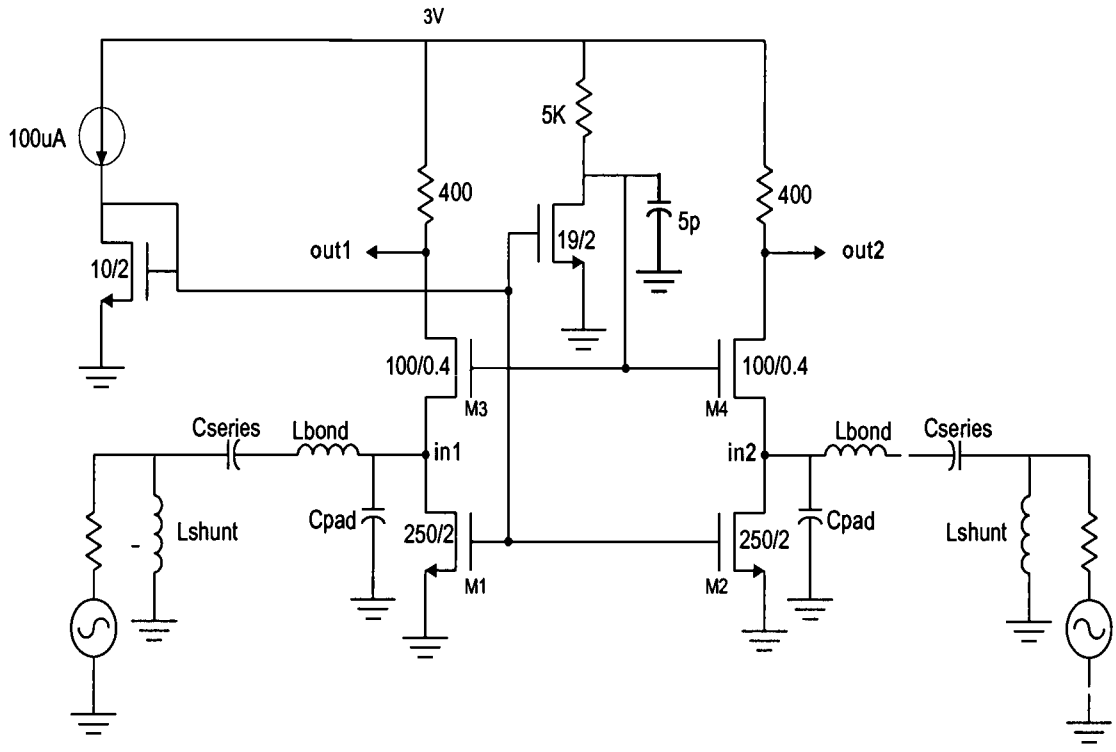

Figure 6-2: Differential LNA design

Gain	14dB*
NF	4.6dB
1-dB Point	-3.6dBm
IIP3	4.4dBm

*differential-differential, 20dB for single-differential

Table 6-2: Differential LNA results

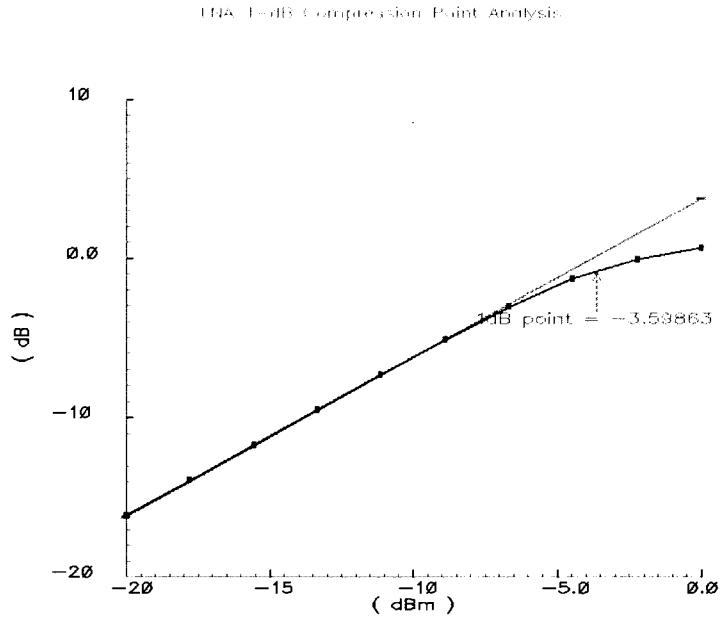

Figure 6-3: LNA 1-dB point from Cadence SpectreRF

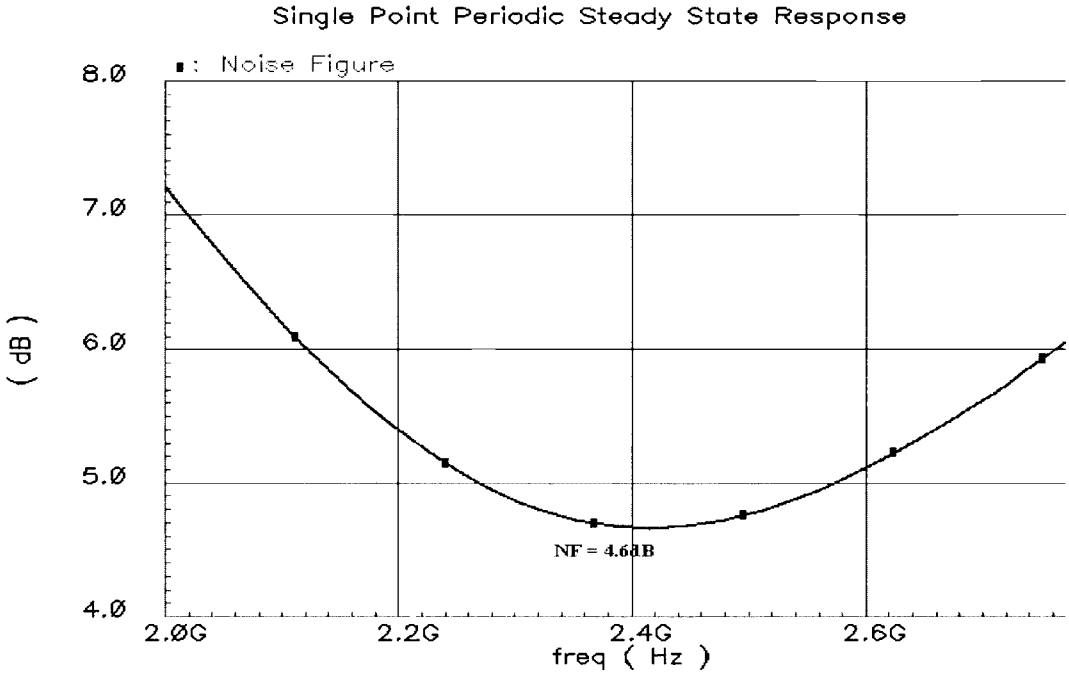

Figure 6-4: NF measurement from PSS analysis

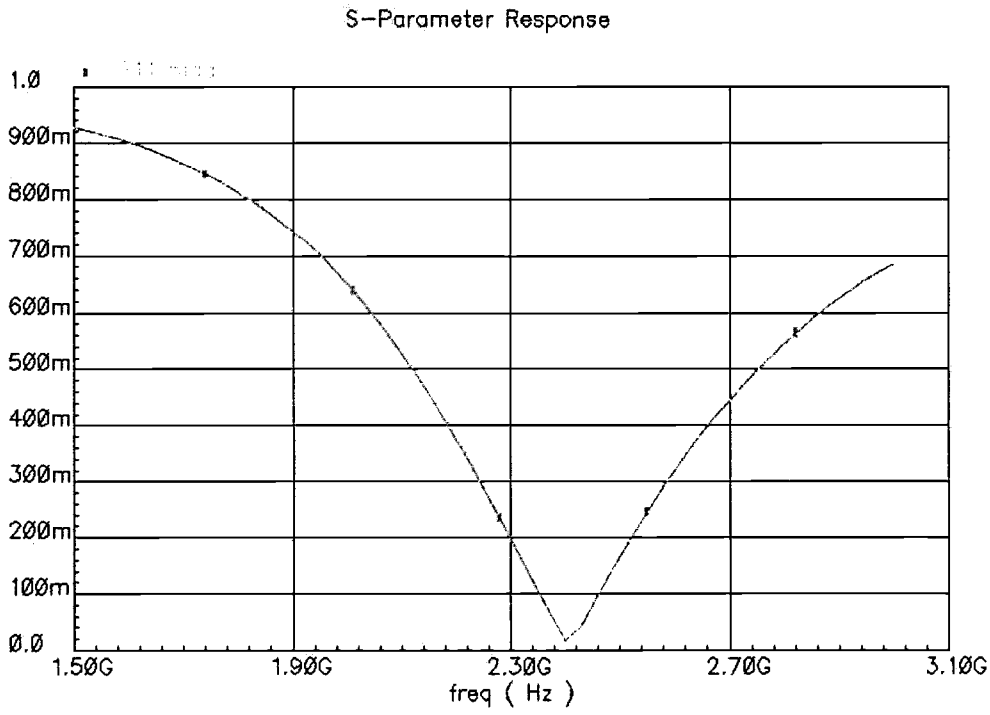

Figure 6-5: S11 measurement from SP analysis in SpectreRF

When cost is the most critical design criteria, it is desired to have an LNA that performs single-to-differential conversion. The 0-180° phase splitter required for a fully differential LNA is commonly placed off-chip before the LNA. This is an expensive component that can significantly boost the overall cost of the receiver. For low cost, lower performance applications it is desirable to integrate the single-to-differential conversion into the LNA. This cost saving comes at the expensive of higher NF. The schematic in Figure 6-6 shows a two stage single-to-differential LNA. The first stage is a single sided version of the circuitry shown in the fully differential (Figure 6-2). A second stage is added to perform the differential split. The signal from stage one is AC coupled to the second stage through C1, while R3 and R4 provide the bias

voltage for the gates of M6 and M7. M5 provides 2.5mA of tail current to the differential pair. The capacitance at the drain of this device causes out2p not to be exactly 180° out of phase with out2n. A compensation capacitor is added to out2n to balance the circuit in order to achieve an exact 180° phase split. Table 6-3 summarizes the results of this LNA. Figure 6-7 shows the frequency response of the LNA, while Figure 6-8 shows the NF analysis done by PSS. Due to the added circuitry the NF of this LNA is higher than the fully differential LNA. The effectiveness of the differential split at the output of the LNA is shown in Figure 6-9.

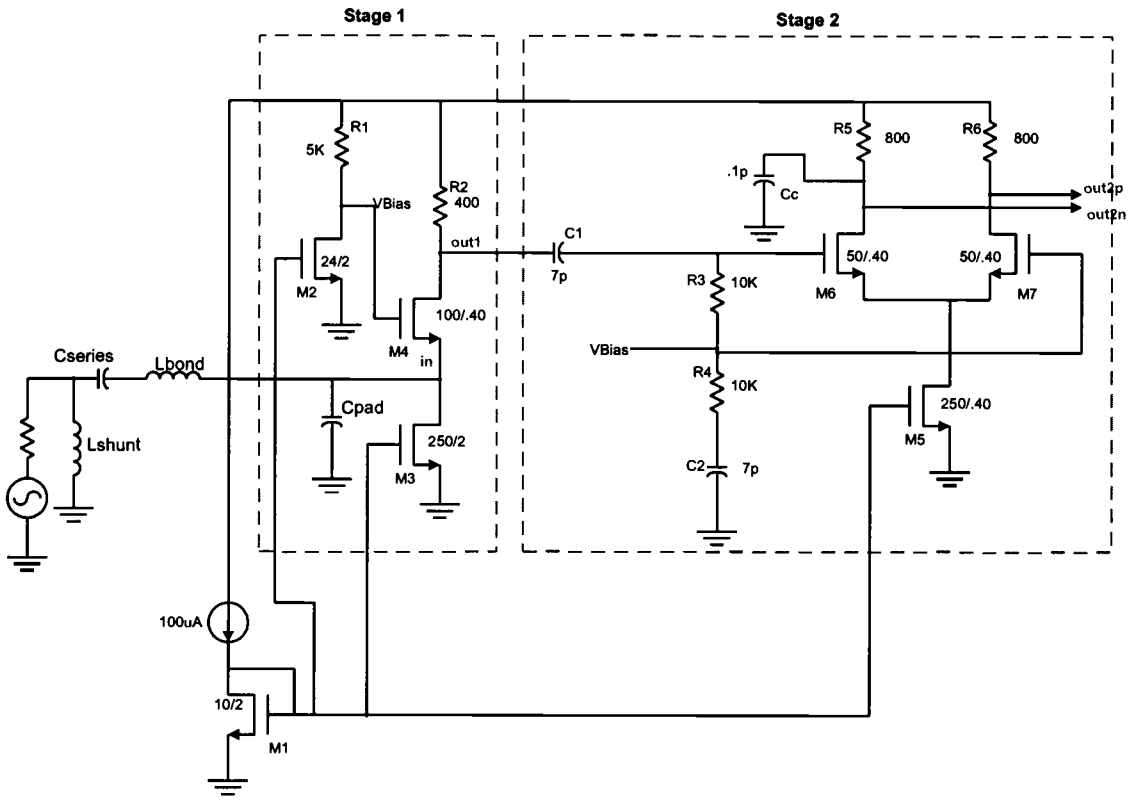

Figure 6-6: Single-to-differential LNA design

Gain	21dB
NF	6.3dB
1-dB Point	-11.3dBm
IIP3	-1.9dBm

Table 6-3: Single-to-differential LNA simulation results

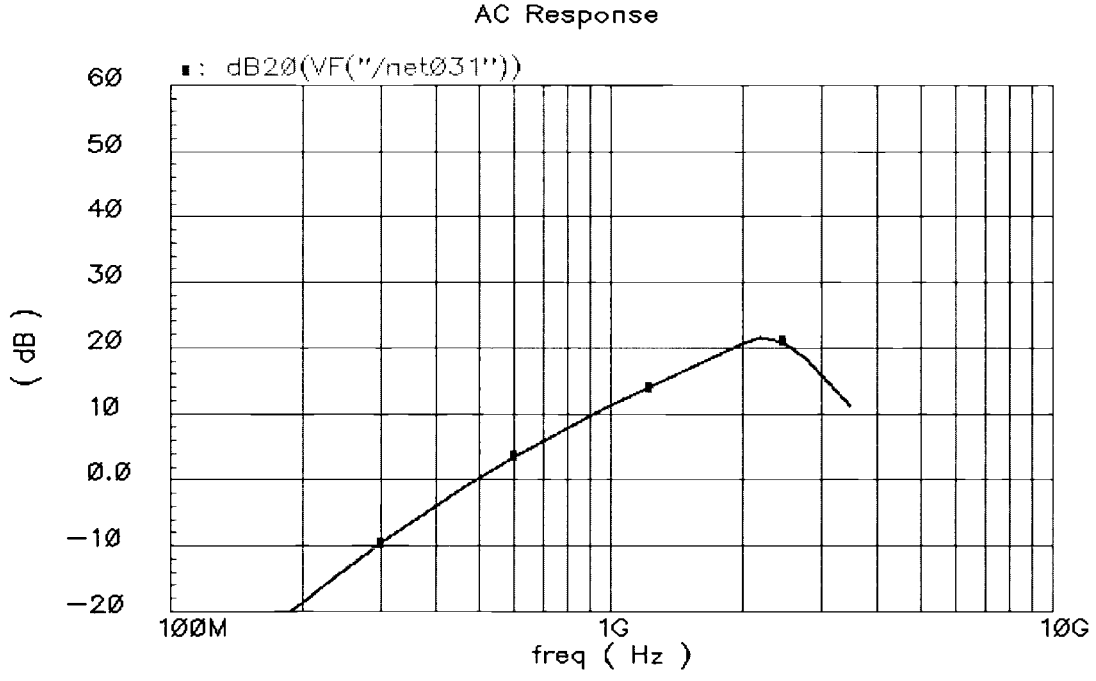

Figure 6-7: Single-to-differential LNA AC response

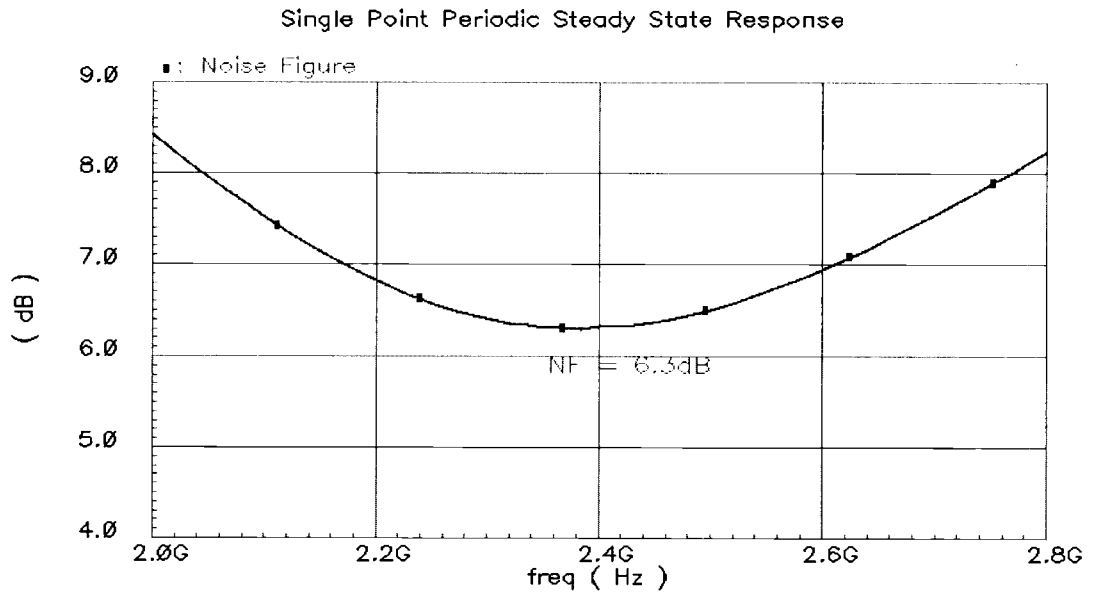

Figure 6-8: NF measurement for single-to-differential LNA using PSS analysis

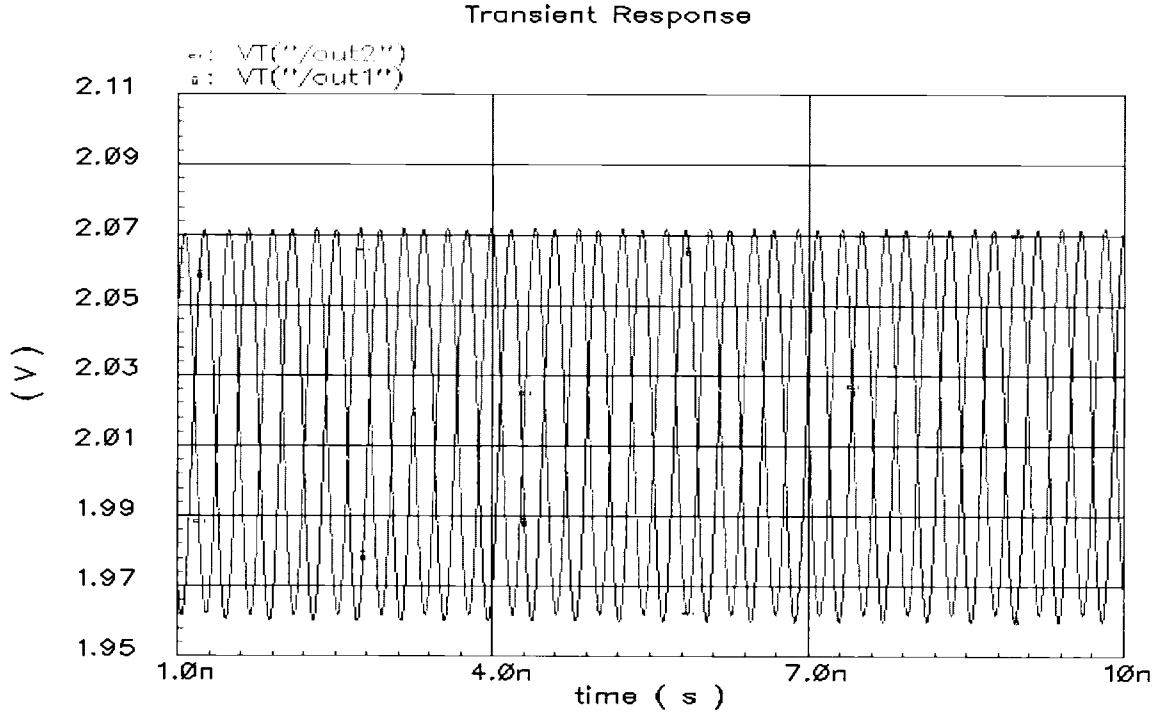

Figure 6-9: Transient response showing single-to-differential split

6.3 Low Pass Filter Design

A LPF is the next block following a mixer in a direct conversion receiver, see Figure 4-1. Their purpose is to adequately reject out-of-channel interferers. Most low pass filters in a direct conversion receiver are active RC filters. They have been shown to have the highest dynamic range over all other active filter implementations and a lower NF than switched capacitor filters with the same power dissipation [8]. Critical to the filter performance is a high gain opamp with low flicker noise. Large input devices and load devices are used to minimize flicker noise in the filter. Even though the signal has seen significant gain in previous stages, noise is still a primary concern in the filter design. If not careful flicker noise from the filter could easily be the dominate noise contributor in the system. Table 6-2 summarizes the results for the opamp used in the RC LPF design.

Gain	60dB
UGBW	25MHz
PM	64.5°
Current	175uA

Table 6-4: Opamp results

The filter is a sixth order modified Sallen-Key type filter (Figure 6-10) [41]. The filter has a bandwidth of 1MHz and rejects the adjacent channel 1MHz away by 45dB. The filter response is shown in Figure 6-11.

The purpose of this filter design is to gain a better understanding of the system design. The opamp and the filter would require additional design/modification before being implemented on-chip.

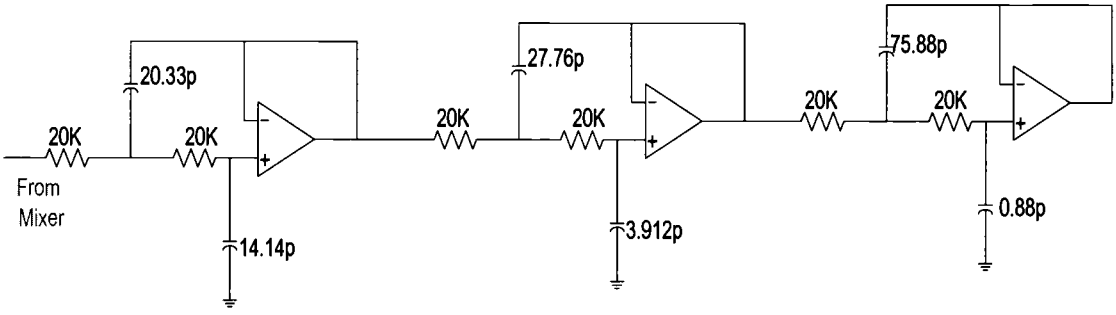

Figure 6-10: LPF design

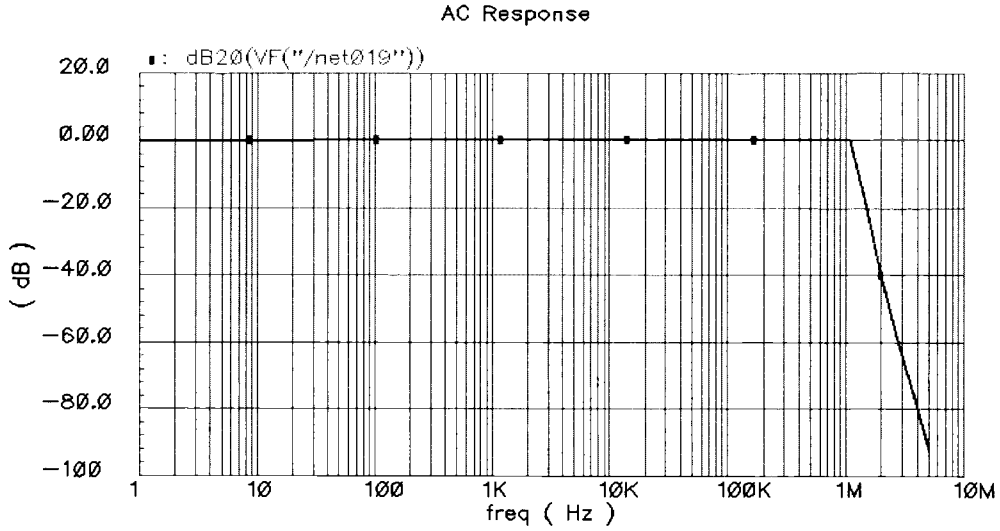

Figure 6-11: Filter response

6.4 System Analysis

The overall system performance is calculated from the individual block performance. Table 6-4 summarized the results from the example front-end design.

	LNA	Mixer	Filter
Gain	20dB	8dB	0dB
IIP3	4.44dBm	17dBm	20dBm
Noise Figure	4.6dB	15dB	34dB

Table 6-5: Front-end prototype results

Using the concepts and equations from Chapter 2, the IIP3 and NF may be calculated for the overall system. With the designed circuits the, overall system SFDR is 64dB (equation 2.7), the Sens is -93.45 (equation 2.6), the IIP3 is –9.2dBm (equation 2.5), and the NF is 8.55dB (equation 2.2). This system meets the specifications for Bluetooth, see Table 6-1. When evaluating the system design and performance, it is useful to demonstrate the performance with a level diagram, as shown in Figure 6-12. The diagram helps to identify which block is limiting the overall dynamic range of the system. The chart shows that the filter is the upper limit on the dynamic range. The IIP3 performance of this filter is less than other published active RC filters by about 10dB. When calculating the upper end of the system dynamic range with a filter IIP3 of 30dBm, the mixer dominates the cascaded IIP3 calculation. Since

the mixer IIP3 limits the top end of the SFDR and its NF is non-dominant, linearity should be the most critical design parameter in mixer design.

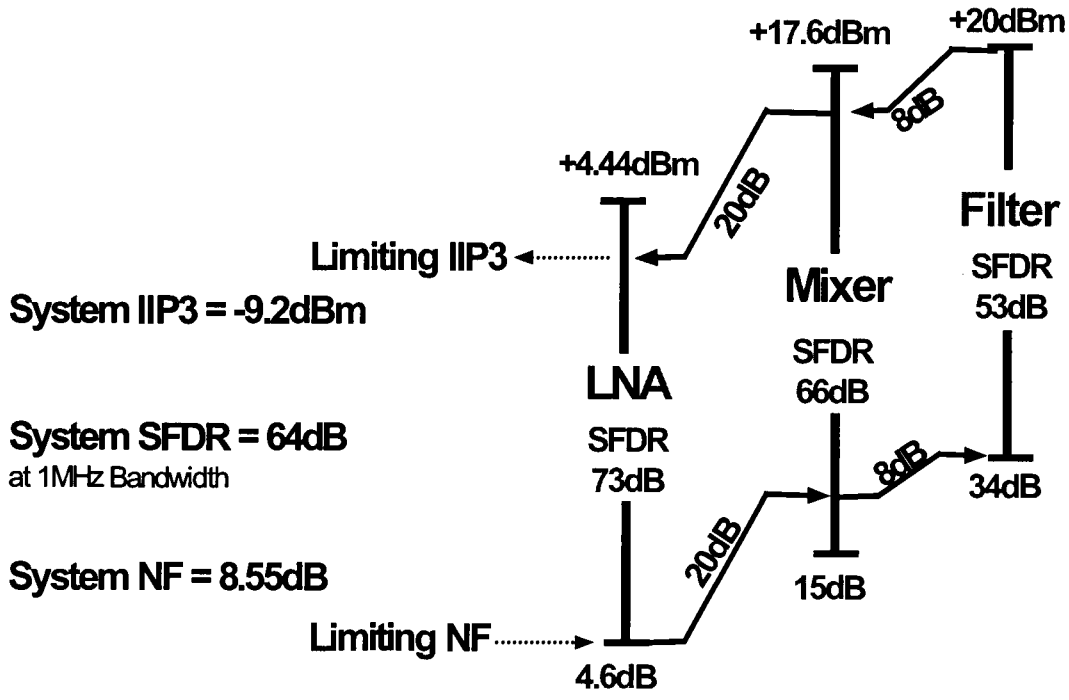

Figure 6-12: System dynamic range

The circuits designed in this research do not match present BICMOS cellular circuits, but they do meet the Bluetooth specifications using a standard CMOS process, which will have a significant cost advantage over current receivers. An inductor-less, fully integrated CMOS receiver could be manufactured for under $2. CMOS receivers may not be used in cell phones anytime soon, but there is a huge market for these type of low cost receivers, i.e., home networking, home control, short- range communication. These markets have not been developed to date because the cost of past receivers made the systems unmarketable.

7.0 CONCLUSION

This work presents a solution to the offset problem associated with direct conversion. The solution is completely integrated to maintain the attractive low cost characteristic of the architecture. Additionally, all circuit solutions are implemented in a standard CMOS process due to its cost effectiveness. A DSP controlling a DAC will adjust the load current of a Gilbert Cell type mixer to create an offset cancellation current. The DAC and mixer designs are presented in this thesis, while the DSP algorithm is presented in [43]. The mixer and DAC were layed out in a TSMC 0.35-um process and fabed by MOSIS. The fabed chip did not work as designed, due to mistakes made with pad placement. Two LNA designs are presented one fully differential and the other single-to-differential. In addition, a Sallen-Key RC LPF was designed to be incorporated with these circuits. A CMOS RF front-end constructed from these circuits will meet the specifications for Bluetooth.

BIBLIOGRAPHY

[1] T. H. Lee, "LNA and Mixer Design," *The Design of CMOS Radio-Frequency Integrated Circuits*. New York, NY: Cambridge University Press, pp.272-340, 1998.

[2] B. Razavi, "Transceiver Architectures, and Low-Noise Amplifiers and Mixers," *RF Microelectronics*. Upper saddle River, NJ: Prentice Hall, pp. 118-200, 1998.

[3] S. A. Maas, "Mixers for Wireless Applications," *RF and Microwave Circuit Design for Wireless Communications*. Norwood, MA: Artech House, pp. 282, 1997.

[4] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. of Solid-State Circuits*, vol. 30, no. 12, pp. 1399-1410, 1995.

[5] B. Razavi, "Challenges in Portable RF Transceiver Design," *Circuits & Devices*, pp. 12-25, Sept. 1996.

[6] P. R. Gray *et al.,* "Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems," *Int. Symp. on Low Power Electronics*, Monterey, Ca, August 1998.

[7] T.H. Lee, H. Samavati, H.R. Rategh, "A 5-GHz CMOS Wirelell LAN Receiver Front End," *IEEE J. of Solid-State Circuits*, vol. 35, no. 5, pp. 765-772, 2000.

[8] H. Darabi, A. Abidi, "A 4.5-mW 900-MHz CMOS Receiver for Wireless Paging," *IEEE J. of Solid-State Circuits*, vol. 35, no. 8, pp. 1085-1096, 2000.

[9] A. Rofougaran, *et al.,* "A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS Part II: Receiver Design," *IEEE J. of Solid-State Circuits*, vol. 33, no. 4, pp. 535-547, 1998.

[10] A. Rofougaran, J. Y-C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver", *IEEE J. of Solid-State Circuits*, vol. 31, no. 7, pp. 880-889, 1996.

[11] T. Cho, et al., "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones", *IEEE International Solid-State Circuits Conference*, pp. 228-229, 1999.

[12] B. Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's," *IEEE J. of Solid-State Circuits*, vol. 34, no. 10, pp. 1382-1385, 1999.

[13] C. D. Hull, J. L. Tham, R. R. Chu, "A Direct-Conversion Receiver for 900MHz (ISM Band) Spread-Spectrum Digital Cordless Telephone", *IEEE J. of Solid-State Circuits*, vol. 31, no. 12, pp. 1955-1963, 1996.

[14] F. Behbahani, J.C. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino, A. Abidi, "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-um CMOS – Architecture and Front-End", *IEEE J. of Solid-State Circuits*, vol. 35, no. 12, pp. 1908-1916, 2000.

[15] F.R. Long, "A Low-Voltage 5.1-5.8-GHz Image-Reject Downconverter RF IC", *IEEE J. of Solid-State Circuits*, vol. 35, no. 9, pp. 1320-1328, 2000.

[16] M.T. Terrovitis, R.G. Meyer, "Intermodulation Distortion in Current-Commutating CMOS Mixers", *IEEE J. of Solid-State Circuits*, vol. 35, no. 10, pp. 1461-1473, 2000.

[17] M. Steyaert, J. Janssens, B. De Muer, M. Borremans, N. Itoh, "A 2-V CMOS Cellular Transceiver Front-End", *IEEE J. of Solid-State Circuits*, vol. 35, no. 12, pp. 1895-1907, 2000.

[18] J. F. Wilson, R. Youell, T. H. Richards, G. Luff, and R. Pilaski, "A Single-Chip VHF and UHF Receiver for Radio Paging," *IEEE J. of Solid-State Circuits*, vol. 26, no. 12, pp. 1944-1950, 1991.

[19] T. Yamaji, H. Tanimoto, H. Kokatsu, "An I/Q Active Balanced Harmonic Mixer with IM2 Cancelers and a 45° Phase Shifter", *IEEE J. of Solid-State Circuits*, vol. 33, no. 12, pp. 2240-2246, 1998.

[20] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, K. Halonen, "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications," *IEEE J. of Solid-State Circuits*, vol. 34, no. 12, pp. 1893-1903, 1999.

[21] C. Takahasi, R. Fujimoto, S. Arai, T. Itakura, T. Ueno, H. Tsurumi, H. Tanimoto, S. Watanabe, K. Hirakawa, "A 1.9GHz Si Direct Coversion Receiver IC for QPSK Modulation Systems," *Int. Solid-State Circuits Conf.,* San Fransico, pp. 139-139, 1995.

[22] B. K. Ko, K. Lee, "A Comparative Study on the Various Monolithic Low Noise Amplifier Circuit Topologies for RF and Microwave Applications," *IEEE J. of Solid-State Circuits*, vol. 31, no. 8, pp. 1220-1225, 1996.

[23] J. C. Rudell, J. Ou, T. B. Cho, G. Chein, F. Brianti, J. A. Weldon, P. R. Gray, "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE J. of Solid-State Circuits*, vol. 32, no. 12, pp. 2071-2088, 1997.

[24] D. K. Shaeffer, *et al.,* "A 115-mW, 0.5-μm CMOS GPS Receiver with Wide Dynamic-Range Active Filters," *IEEE J. of Solid-State Circuits*, vol. 33, no. 12, pp. 2219-2231, 1998.

[25] P. J. Sullivan, W. H. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", *IEEE J. of Solid-State Circuits*, vol. 32, no. 7, pp. 1151-1155, 1997.

[26] J. Chang, A. Abidi, C.R. Viswanathan, "Flicker Noise in CMOS Transistors from Subthreshold to Strong Inversion at Various Temperatures", *IEEE J. of Solid-State Circuits*, vol. 41, no. 11, pp. 1965-1971, 1994.

[27] Q. Huang, F. Piazza, P. Orsatti, T. Ohguro, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits", *IEEE J. of Solid-State Circuits*, vol. 33, no. 7, pp. 1023-1036, 1998.

[28] M. Terrovitis, R. G. Meyer, "Noise in Current-Commutating CMOS Mixers," *IEEE J. of Solid-State Circuits*, vol. 34, no. 6, pp. 772-783, 1999.

[29] T. H. Lee et al., "A 1GHz Image-Rejection Down-Converter in 0.8um CMOS Technology", *IEEE Transactions on Consumer Electronics,* vol. 44, no. 2, pp. 235-239, 1998

[30] H. Darabi, A.A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model", *IEEE J. of Solid-State Circuits*, vol. 35, no. 1, pp. 15-25, 2000.

[31] T. Manku, "Microwave CMOS – Device Physics and Design", *IEEE J. of Solid-State Circuits*, vol. 34, no. 3, pp. 277-285, 1999.

[32] B. Razavi, "CMOS Technology Characterization for Analog and RF Design", *IEEE J. of Solid-State Circuits*, vol. 34, no. 3, pp. 268-275, 1999.

[33] J. Sullivan, "Single-Chip Solutions Target Bluetooth Applications", *Wireless Design Online*, Vertical Net, 2000

[34] P. Kan, K. Hoch, "Si Requirements Challenge Bluetooth Vendors", *Wireless Systems Design*, pp. 33-36, February, 2000.

[35] R. Schneiderman, "Bluetooth Projections Push Product Development", *Wireless Systems Design,* pp. 9-14, Winter Issue 2000.

[36] B. Kyu Ko, and K. Lee, "A Comparative Study on the Various Monolithic Low Noise Circuit Topologies for RF and Microwave Applications", *IEEE J. of Solid-State Circuits*, vol. 31, no. 8, pp. 1220-1225, 1996.

[37] Q. Huang, P. Orsatti, F. Piazza, "GSM Transceiver Front-End Circuits in 0.25-um CMOS", *IEEE J. of Solid-State Circuits*, vol. 34, no. 3, pp. 292-303, 1999.

[38] D. Shaeffer, T. H. Lee, "A 1.5-V, 1.5GHz CMOS Low Noise Amplifier," *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, 1997.

[39] J. Chang, *An Integrated 900MHz Spread-Spectrum Wireless Receiver in 1-um CMOS and a Suspended Inductor Technique*, Ph.D. Thesis, University of California-Los Angeles, Department of Electrical Engineering, 1998.

[40] J. Stonick, "Wireless Communications System Design", Oregon State University ECE 663, 2000.

[41] A. Williams, and F. Taylor, "Low Pass Filter Design", *Electronic Filter Design Handbook.* San Francisco, CA McGraw-Hill Inc., pp. 3.15-3.46, 1995.

[42] Bluetooth Special Interest Group, "Radio Specification", Version 1.0 B, July 2000, available via web site at http:\\www.bluetooth.com\developer\specification\specification.asp.

[43] C. Holenstein, *Adaptive-Dual-Loop Algorithm for Cancellation of Time-Varying Offsets in Direct Conversion Mixers*, MS Thesis, Oregon State University, Department of Electrical and Computer Engineering, March 12, 2001.

[44] B. Gilbert, "A Precise Four Quadrant Multiplier with Sub Nanosecond Response," *IEEE Journal of Solid-State Circuits*, pp. 365-373, Dec. 1968.

[45] M. Scarpa, *New Results for Differentially Detected π/4 DQPSK Signal in a Direct Conversion Transceiver*, Oregon State University, Department of Electrical and Competer Engineering, 1998.